


	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	M.E.	Programme Code	203	Regulation	2013
Department	APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING				
CURRICULUM (Applicable to the students admitted from the academic year 2013-2014 onwards)					



SEMESTER – I								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13MA102	Applied Mathematics	3	1	0	4	50	50	100
P13VD101	Solid State Device Modeling and Simulation	3	1	0	4	50	50	100
P13AE101	Advanced Microprocessors and Microcontrollers	3	0	0	3	50	50	100
P13VD103	VLSI Design Techniques	3	0	0	3	50	50	100
P13AE102	Advanced Digital System Design	3	0	0	3	50	50	100
P13VD104	DSP Integrated Circuits	3	0	0	3	50	50	100
PRACTICAL								
P13AE103	Electronics Design Lab I	0	0	3	2	50	50	100
		Total Credits			22	350	350	700

CA - Continuous Assessment, ESE - End Semester Examination

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SEMESTER – II								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13AE204	Analysis and Design of Analog Integrated Circuits	3	0	0	3	50	50	100
P13AE205	Digital Control Engineering	3	0	0	3	50	50	100
P13AE206	Power Electronics	3	0	0	3	50	50	100
P13AE207	Embedded Systems	3	0	0	3	50	50	100
	Elective-I	3	0	0	3	50	50	100
	Elective-II	3	0	0	3	50	50	100
PRACTICAL								
P13AE208	Electronics Design Lab II	0	0	3	2	50	50	100
		Total Credits			20	350	350	700

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SEMESTER – III								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
	Elective-III	3	0	0	3	50	50	100
	Elective-IV	3	0	0	3	50	50	100
	Elective-V	3	0	0	3	50	50	100
PRACTICAL								
P13AE309	Project Work(Phase I)	0	0	12	6	50	50	100
		Total Credits			15	200	200	400

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SEMESTER – IV								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
PRACTICAL								
P13AE410	Project Work (Phase II)	0	0	24	12	50	50	100
		Total Credits			12	50	50	100

CA - Continuous Assessment, ESE - End Semester Examination

LIST OF ELECTIVES



Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13AEE01	Digital Image Processing	3	0	0	3	50	50	100
P13AEE02	Neural Networks and Its Applications	3	0	0	3	50	50	100
P13AEE03	Robotics	3	0	0	3	50	50	100
P13AEE04	Design and Analysis of Algorithms	3	0	0	3	50	50	100
P13AEE05	Reliability Engineering	3	0	0	3	50	50	100
P13AEE06	Electromagnetic Interference and Compatibility in System Design	3	0	0	3	50	50	100
P13AEE07	RF System Design	3	0	0	3	50	50	100
P13AEE08	Hardware Software Co-Design	3	0	0	3	50	50	100
P13AEE09	Nano Electronics	3	0	0	3	50	50	100
P13VDE06	ASIC Design	3	0	0	3	50	50	100
P13VD207	Low Power VLSI Design	3	0	0	3	50	50	100
P13VD208	VLSI Signal Processing	3	0	0	3	50	50	100
P13VDE02	Analog VLSI Design	3	0	0	3	50	50	100
P13VD206	CAD for VLSI Circuits	3	0	0	3	50	50	100
P13AEE09	High Performance Computer Networks	3	0	0	3	50	50	100
P13CSE08	Computer Architecture and Parallel Processing	3	0	0	3	50	50	100

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Programme	M.E.	Programme Code		Regulation	2013
Department	VLSI DESIGN , POWER SYSTEMS & APPLIED ELECTRONICS			Semester	I

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13MA102	APPLIED MATHEMATICS	3	1	0	4	50	50	100

Objectives	<ul style="list-style-type: none"> • At the end of the course Student would be exposed to fundamental knowledge in • One Dimensional random variables, Testing the hypothesis • Linear programming, Computational methods in Engineering and • Various Queuing models. 							
Unit – I	ONE DIMENSIONAL RANDOM VARIABLE					Periods	9+3	
Random Variables- Probability Function-Moments-Moment Generating Function & their Properties- Binomial, Poisson, Geometric, Uniform, Exponential Distributions:								
Unit – II	TESTING OF HYPOTHESIS					Periods	9+3	
Basic Definitions:- (Population, Sampling, Tests of Significance, Testing a Hypothesis, Null Hypothesis, Alternative Hypothesis, Level of Significance, Types of Errors) – Testing of Hypothesis using : ‘t’-Test , ‘F’-Test , Chi Square Test (χ^2) - Test for Independence of Attributes & Goodness of Fit								
Unit – III	LINEAR PROGRAMMING					Periods	9+3	
Formulation-Graphical solution-Simplex Method -Transportation and Assignment problems.								
Unit – IV	DYNAMIC PROGRAMMING					Periods	9+3	
Dynamic Programming-principle of optimality-forward and backward recursion-DP Applications (Cargo loading method)-Problems of dimensionality.								
Unit – V	QUEUING MODELS					Periods	9+3	
Introduction-Markovian Models: M/M/1: infinite capacity-M/M/C: infinite capacity-M/M/1: finite capacity – M/M/C : finite capacity, Little’s formula.								
						Total Periods	60	
REFERENCES:								
1.	B.V.Ramana – ‘Higher Engineering Mathematics’, by Tata Mc Graw Hill Publishing Pvt Ltd – New Delhi, 2008 th Edition.							
2.	Taha,H.a., Operations Research: An Introduction,seventh Edition,Person Education edition,Asia,New Delhi(2002).							



3.	Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000
4.	Donald Gross and Carl M. Harris, Fundamentals of queuing theory, 2 nd edition, John Wiley and Sons, New York (1985)
5.	Richard Johnson, Miller & Freund's probability and statistics for engineers, 7 th edition, Prentice-Hall of India, Private Ltd., New Delhi (2007)

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	I

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD101	SOLID STATE DEVICE MODELING AND SIMULATION	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To study and model MOSFET and advanced MOSFET To Model the Process Variation and quality assurance 							
Unit – I	MOSFET DEVICE PHYSICS					Periods	9	
MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.								
Unit – II	NOISE MODELING					Periods	9	
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.								
Unit – III	BSIMV4 MOSFET MODELING					Periods	9	
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitic model.								
Unit – IV	OTHER MOSFET MODELS					Periods	9	
The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model.								
Unit – V	MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE					Periods	9	
Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests.								
						Total Periods	45	
REFERENCES:								
1.	Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2003.							

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| 2. | Christian C. Enz, Eric A. Vittoz, "Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design", John Wiley & Sons, Ltd, 2006. |
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Department	APPLIED ELECTRONICS & VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	I

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE101	ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS	3	0	0	3	50	50	100



Objectives	<ul style="list-style-type: none"> To introduce the concepts of advanced microprocessors. To provide an in-depth knowledge about microprocessor architecture To familiarize the basic architecture of Pentium family of processors. To know about the inner workings of the 68HC11 microprocessor To understand the essentials of PIC microcontrollers design and programming using assembly language. 							
Unit – I	MICROPROCESSOR ARCHITECTURE					Periods	9	
Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline– pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.								
Unit – II	HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM					Periods	9	
CPU Architecture- Bus Operations – Pipelining – Branch predication – floating point unit- Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.								
Unit – III	HIGH PERFORMANCE RISC ARCHITECTURE – ARM					Periods	9	
Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.								
Unit – IV	MOTOROLA 68HC11 MICROCONTROLLERS					Periods	9	
Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.								
Unit – V	PIC MICROCONTROLLER					Periods	9	
CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.								
						Total Periods	45	

REFERENCES:

1.	Daniel Tabak , “ Advanced Microprocessors” McGraw Hill.Inc., 1995
2.	James L. Antonakos , “ The Pentium Microprocessor “ Pearson Education ,1997.

FURTHER READINGS:

1.	Steve Furber , “ ARM System –On –Chip architecture “Addision Wesley , 2000.
2.	Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003. John .B.Peatman
3.	John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
4.	John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	I

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD103	VLSI DESIGN TECHNIQUES	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To Understand the concepts of NMOS and PMOS transistors To Understand the Basic CMOS technology To Study the Multiplexers To understand the concepts of Basics of CMOS testing. To Understand the concepts of digital design with Verilog HDL 							
Unit – I	MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY					Periods	9	
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.								
Unit – II	INVERTERS AND LOGIC GATES					Periods	9	
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.								
Unit – III	CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION					Periods	9	
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.								
Unit – IV	VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN					Periods	9	
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.								
Unit – V	VERILOG HARDWARE DESCRIPTION LANGUAGE					Periods	9	



Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

Total Periods

45

REFERENCES:

1.	Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2 nd edition, 2000.
2.	John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
3.	Samir Palnitkar, “Verilog HDL”, Pearson Education, 2 nd Edition, 2004.
4.	Eugene D.Fabircius, Introduction to VLSI Design McGraw Hill International Editions, 1990.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE102	ADVANCED DIGITAL SYSTEM DESIGN	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To provide an in-depth knowledge of synchronous and asynchronous sequential circuits analysis and design To provide the basics of fault diagnosis and testing algorithms To study the design of synchronous sequential circuits using PLDs To study the design of digital systems using VHDL 							
Unit - I	SEQUENTIAL CIRCUIT DESIGN					Periods	9	
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits -design of iterative circuits-ASM chart and realization using ASM								
Unit - II	ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN					Periods	9	
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.								
Unit - III	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS					Periods	9	
Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test								
Unit - IV	SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES					Periods	9	
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000								
Unit - V	SYSTEM DESIGN USING VHDL					Periods	9	
VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.								

		Total Periods	45
REFERENCES:			
1.	Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004		
FURTHER READINGS:			
1.	Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001		
2.	Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002		
3.	Parag K.Lala “Digital system Design using PLD” B S Publications,2003		
4.	Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004		
5.	Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill – 2006		



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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD104	DSP INTEGRATED CIRCUITS	3	1	0	4	50	50	100

Objectives	<ul style="list-style-type: none"> To study the advanced digital signal processors and IC technologies. To explore the concepts of multi rate signal processing and multi rate filters. To study the complex multipliers and VLSI layouts. 							
Unit – I	DSP INTEGRATED CIRCUITS & VLSI CIRCUIT TECHNOLOGIES					Periods	9	
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.								
Unit – II	DIGITAL SIGNAL PROCESSING					Periods	9	
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.								
Unit – III	DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS					Periods	9	
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.								
Unit – IV	DSP ARCHITECTURES & SYNTHESIS OF DSP ARCHITECTURES					Periods	9	
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputer, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.								

Unit – V	SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS	Periods	9
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. CORDIC algorithm.			
		Total Periods	45
REFERENCES:			
1.	Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York 1999		
2.	Oppenheim A.V. et.al, ‘Discrete-time Signal Processing’ Pearson education,2000		
FURTHER READINGS:			
1.	Emmanuel C. Ifeachor, Barrie W. Jervis, “ Digital signal processing – A practical approach”, Second edition, Pearson education, Asia 2001 practical approach”, Second edition, Pearson education, Asia 2001		
2.	Keshab K.Parhi, ‘VLSI digital Signal Processing Systems design and Implementation’ John Wiley & Sons, 1999		



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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE103	ELECTRONIC DESIGN LAB I	0	0	3	2	50	50	100

LIST OF EXPERIMENTS:

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16- bit Microprocessor.



TOTAL PERIODS : 60 HOURS

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE204	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To provide an in-depth knowledge in computer fundamentals. To provide the basics of C programming language. To enhance the fundamental Application relevant to C programming language. 			
Unit – I	MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES	Periods	9	
Depletion region of PN junction– Large signal behavior of Bipolar Transistors–small signal model of bipolar transistors – large signal behavior of MOSFET – small signal of MOS transistors – short channel effects in MOS transistors– Weak inversion in MOS transistors – substrate current flow in MOS transistor.				
Unit – II	CIRCUIT CONFIGURATION FOR LINEAR IC	Periods	9	
Current sources, Analysis of differential amplifiers with active load using BJT and FET, supply and temperature independent biasing technique, voltage references, output stages: current follower, source follower and push pull output stages.				
Unit – III	OPERATIONAL AMPLIFIERS	Periods	9	
Analysis of operational amplifier circuit, slew rate model and high frequency analysis, frequency response of integrated circuits: single stage and multistage amplifier and operational amplifiers noise.				
Unit – IV	ANALOG MULTIPLIER AND PLL	Periods	9	
Analysis of four quadrants and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL-monolithic PLL design in integrated circuits: Sources of noise-noise model of integrated circuit components-circuit noise calculations-equivalent noise input generators-noise bandwidth-noise figure and noise temperature.				
Unit – V	ANALOG DESIGN WITH MOS TECHNOLOGY	Periods	9	
Mos current mirrors-simple, cascade, Wilson and widlar current sources-CMOS class AB output stages-two stage MOS operational amplifiers, with cascade, telescopic-cascade operational amplifiers-MOS folded cascade and MOS active cascade operational amplifiers.				
			Total Periods	45

REFERENCES:	
1.	Gray, Meyer, Lewis and Hurst, "Analysis and design of analog ICs", Fourth Edition, Willey International, 2002
2.	Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
FURTHER READINGS:	
1.	Nandita Dasgupta, Amitava Dasgupta, "Semiconductor devices , modeling and technology", Prentice Hall of India Pvt Ltd, 2004
2.	Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley and sons. Inc. 2003
3.	Phillip. E. Allen Douglas R Holberg , CMOS Analog Integrated circuit design", second edition – Oxford University Press. 2003

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE205	DIGITAL CONTROL ENGINEERING	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To understand different types of controllers To enhance sampling techniques Design of different digital control algorithms 							
Unit – I	PRINCIPLES OF CONTROLLERS					Periods	9	
Review of frequency and time response analysis and specifications of control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers								
Unit – II	SIGNAL PROCESSING IN DIGITAL CONTROL					Periods	9	
Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.								
Unit – III	MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM					Periods	9	
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.								
Unit – IV	DESIGN OF DIGITAL CONTROL ALGORITHMS					Periods	9	
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.								
Unit – V	PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS					Periods	9	
Algorithm development of PID control algorithms, software implementation, Implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.								
						Total Periods	45	

REFERENCES:

1.	M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, NewDelhi, 1997.
2.	John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,



	1995.
3.	Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

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Programme	M.E.	Programme Code	203	Regulation	2013
Department	APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		II

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE206	POWER ELECTRONICS	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To get an overview of different types of power semi-conductor devices and their switching characteristics. To understand the operation, characteristics and performance parameters of controlled rectifiers. To study the operation, switching techniques and basic topologies of DC-DC switching regulators. To learn the different modulation techniques of pulse width modulated inverters and to understand the harmonic reduction methods. To study the operation of AC voltage controller and Matrix converters. To study simple applications. 							
Unit - I	POWER SEMI-CONDUCTOR DEVICES				Periods	12		
Study of switching devices, - Frame, Driver and snubber circuit of SCR, TRIAC, BJT, IGBT, MOSFET, - Turn-on and turn-off characteristics, switching losses, Commutation circuits for SCR.								
Unit - II	PHASE-CONTROLLED CONVERTERS				Periods	12		
Bipolar transistor action, minority carrier distribution, low frequency common-base current gain, non ideal effects, equivalent circuit models, frequency limitations, large signal switching.								
Unit - III	DC TO DC CONVERTER				Periods	12		
Step-down and step-up chopper - Time ratio control and current limit control – Buck, boost, buck-boost converter, concept of Resonant switching - SMPS.								
Unit - IV	INVERTERS				Periods	12		
Single phase and three phase (both 120° mode and 180° mode) inverters - PWM techniques: Sinusoidal PWM modified sinusoidal PWM - multiple PWM – Introduction to space vector modulations - Voltage and harmonic control - Series resonant inverter - Current source inverter.								
Unit - V	AC To AC CONVERTERS				Periods	12		
Single phase AC voltage controllers – Multistage sequence control - single and three phase cycloconverters – Introduction to Integral cycle control, Power factor control and Matrix converters.								
					Total Periods	60		
REFERENCES:								

1.	M.H. Rashid, 'Power Electronics: Circuits, Devices and Applications', Pearson Education, PHI Third edition, New Delhi 2004.
2.	Philip T.Krein, "Elements of Power Electronics" Oxford University Press, 2004 Edition.
FURTHER READINGS:	
1.	Ashfaq Ahmed Power Electronics for Technology Pearson Education, Indian reprint, 2003.
2.	P.S.Bimbra "Power Electronics" Khanna Publishers, third Edition 2003.
3.	Ned Mohan, Tore.M.Undeland, William.P.Robbins, 'Power Electronics: Converters, Applications and Design', John Wiley and sons, third edition, 2003.



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Programme	M.E.	Programme Code		Regulation	2013
Department	APPLIED ELECTRONICS & VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	II

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE207	EMBEDDED SYSTEMS	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To provide an in-depth knowledge of embedded system. To provide the basics of embedded processor. To study the design of embedded processor and computing platform. To study the design of networks. 							
Unit – I	EMBEDDED PROCESSORS					Periods	9	
Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller, ARM processor processor and memory organization.								
Unit - II	EMBEDDED PROCESSOR AND COMPUTING PLATFORM					Periods	9	
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture.								
Unit - III	NETWORKS					Periods	9	
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design-Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.								
Unit - IV	REAL-TIME CHARACTERISTICS					Periods	9	
Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.								
Unit – V	SYSTEM DESIGN TECHNIQUES					Periods	9	
Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.								

REFERENCES:

1.	Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers.
2.	Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia.
3.	C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997
4.	Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons.



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Programme	M.E.	Programme Code	203	Regulation	2013
Department	APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		II

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE208	ELECTRONICS DESIGN LAB -II	0	0	3	2	50	50	100

LIST OF EXPERIMENTS:

1. System design using PLL.
2. System design using CPLD.
3. Alarm clock using embedded micro controller.
4. Model train controller using embedded micro controller.
5. Elevator controller using embedded micro controller.
6. Simulation of Non adaptive Digital Control System using MAT LAB control system Toolbox.
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.



TOTAL PERIODS : 45 HOURS

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Department	APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE01	DIGITAL IMAGE PROCESSING	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To study the fundamentals of digital image and to understand mathematically the various image transform techniques. To study about various image enhancement and restoration techniques. To learn about image segmentation and recognition schemes. To understand the need for image compression and study various compression techniques. 							
Unit - I	DIGITAL IMAGE FUNDAMENTALS				Periods	9		
Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries								
Unit - II	IMAGE TRANSFORMS				Periods	9		
1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.								
Unit - III	IMAGE ENHANCEMENT AND RESTORATION				Periods	9		
Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic and Yp mean filters, Design of 2D FIR filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray Level interpolation.								
Unit - IV	IMAGE SEGMENTATION AND RECOGNITION				Periods	9		
Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Back propagation network and training, Neural network to recognize shapes.								
Unit - V	IMAGE COMPRESSION				Periods	9		
Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.								



		Total periods	45
REFERENCES:			
1.	Dr.S.Jayaraman, Digital Image Processing TMH New Delhi ,2009		
2.	Rafael C- Gonzalez- Richard E-Woods- 'Digital Image Processing' - Pearson Education- Inc-- Second Edition- 2004		
3.	Anil K- Jain- 'Fundamentals of Digital Image Processing' - Pearson/Prentice Hall of India- 2002		
FURTHER READING:			
1.	Rafael C. Gonzalez, Richard E. Woods, Steven Eddins," Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.		
2.	D.E. Dudgeon and R.M. Mersereau, "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.		
3.	William K-Pratt- 'Digital Image Processing'- John Wiley- NewYork- 2002		
4.	Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;		
5.	Sid Ahmed, M.A., " Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.		

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Department	APPLIED ELECTRONICS & VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE16	NEURAL NETWORKS AND ITS APPLICATIONS	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To study the basic network learning algorithms To understand the concept of radial basis networks and functions To study committee machines and neurodynamics systems To study attractor neural networks and adaptive resonance theory To understand the concept of self organizing maps and pulsed neuron models 							
Unit - I	BASIC LEARNING ALGORITHMS					Periods	9	
<p>Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feed forward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering-Beam forming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.</p>								
Unit - II	RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES RADIAL BASIS FUNCTION NETWORKS					Periods	9	
<p>Cover's Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification. Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - - insensitive Loss Function – Support Vector Machines for Nonlinear Regression.</p>								
Unit - III	COMMITTEE MACHINES					Periods	9	
<p>Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model</p>								



NEURODYNAMICS SYSTEMS:			
Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems- Lyapunov Stability – Neurodynamical Systems – The Cohen-Grossberg Theorem.			
Unit - IV	ATTRACTOR NEURAL NETWORKS	Periods	9
Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications			
ADAPTIVE RESONANCE THEORY:			
Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center – Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications			
Unit - V	SELF ORGANISING MAPS	Periods	9
Self-organizing Map – Maximal Eigenvector Filtering – Sanger’s Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications			
PULSED NEURON MODELS:			
Spiking Neuron Model – Integrate-and-Fire Neurons – Conductance Based Models – Computing with Spiking Neurons			
		Total Periods	45
REFERENCES:			
1.	Satish Kumar, “Neural Networks: A Classroom Approach”, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.		
2.	Simon Haykin, “Neural Networks: A Comprehensive Foundation”, 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.		
3.	Martin T.Hagan, Howard B. Demuth, and Mark Beale, “Neural Network Design”, Thomson Learning, New Delhi, 2003.		
4.	James A. Freeman and David M. Skapura, “Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.		

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE02	ROBOTICS	3	0	0	3	50	50	100



Objectives	<ul style="list-style-type: none"> To study the CMOS & BiCMOS design circuits To understand sampled data filter and sensor. To derive First-order and Second SC Circuits equations. 		
Unit - I	BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW- VOLTAGE SIGNAL PROCESSING	Periods	9
Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.			
Unit - II	BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING	Periods	9
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired.			
Unit - III	SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS	Periods	9
First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched- Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters- Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma- Delta Modulators-Interpolative Modulators – Cascaded Architecture-Decimation Filters- Sensors-Sensor Interfaces.			
Unit - IV	DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS	Periods	9
Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron -Beam Testability.			

Unit - V	STATISTICAL MODELING AND SIMULATION,ANALOG COMPUTER- AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT	Periods	9
Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.			
		Total Periods	45
REFERENCES:			
1.	Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw- Hill International Editons, 1994		
2.	Malcom R.Haskard, Lan C.May, "Analog VLSI Design - NMOS and CMOS ",PrenticeHall, 1998		
3.	Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990		
4.	Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994		

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Programme	M.E.	Programme Code	203	Regulation	2013
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P		C	CA	ESE
P13AEE03	DESIGN AND ANALYSIS OF ALGORITHMS	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To study in depth about different types of design techniques of different algorithms. To study different types of searching and sorting algorithms. To study and analysis the graph theory based algorithms for specific applications. 							
Unit - I	INTRODUCTION				Periods	9		
Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.								
Unit - II	DESIGN TECHNIQUES				Periods	9		
Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.								
Unit - III	SEARCHING AND SORTING				Periods	9		
Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior.								
Unit - IV	GRAPH ALGORITHMS				Periods	9		
Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, ax-flow min cut theorem, Steiglitz's link deficit algorithm.								
Unit - V	SELECTED TOPICS				Periods	9		
NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.								
					Total Periods	45		
REFERENCES:								
1.	Sara Baase, "Computer Algorithms: Introduction to Design and Analysis", Addison Wesley, 1988.							
2.	T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.							
3.	E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.							
4.	D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989							



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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE04	RELIABILITY ENGINEERING	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> • Apply engineering knowledge to prevent or reduce frequency of failures • Identify and correct the causes of the failures • Define methods to mitigate the failures that occur if their causes have not been corrected • Apply techniques to estimate the reliability of new designs and analyze reliability data 							
Unit - I	PROBABILITY PLOTTING AND LOAD-STRENGTH				Periods	9		
Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.								
Unit - II	RELIABILITY PREDICTION, MODELLING AND DESIGN				Periods	9		
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.								
Unit - III	ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY				Periods	9		
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.								
Unit - IV	RELIABILITY TESTING AND ANALYSIS				Periods	9		
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.								
Unit - V	MANUFACTURE AND RELIABILITY MAQNAGEMENT				Periods	9		
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.								

REFERENCES:



1.	Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2.	David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3.	Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000
4.	Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE05	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To study the Electromagnetic Interference concepts, coupling principles and Control Techniques. To design PCB for Electromagnetic compatibility. To study instruments and measurements for Electromagnetic Interference. 							
Unit - I	EMI/EMC CONCEPTS				Periods	9		
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.								
Unit - II	EMI COUPLING PRINCIPLES				Periods	9		
Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.								
Unit - III	EMI CONTROL TECHNIQUES				Periods	9		
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.								
Unit - IV	EMC DESIGN OF PCBs				Periods	9		
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.								
Unit - V	EMI MEASUREMENTS AND STANDARDS				Periods	9		
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.								
					Total Periods	45		
REFERENCES:								
1.	V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.							
2.	Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.							
3.	Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3 rd Ed, Artech house, Norwood,							

	1986.
4.	C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
5.	Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.



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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE06	RF SYSTEM DESIGN	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To Understand the concepts of transceivers and its architectures To Understand the impedance matching and amplifiers To Study the feedback system and power amplifiers To Understand the concepts of PLL and Frequency Synthesizers To Learn the process of mixers and oscillators 							
Unit - I	CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES					Periods	9	
<p>CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion , Two step up conversion.</p>								
Unit - II	IMPEDANCE MATCHING AND AMPLIFIERS					Periods	9	
<p>S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.</p>								
Unit - III	FEEDBACK SYSTEMS AND POWER AMPLIFIERS					Periods	9	
<p>Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearisation Techniques – Efficiency boosting techniques – ACPR metric – Design considerations.</p>								
Unit - IV	PLL AND FREQUENCY SYNTHESIZERS					Periods	9	
<p>PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers.</p>								
Unit - V	MIXERS AND OSCILLATORS					Periods	9	
<p>Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – sub sampling mixers Oscillators: Describing Functions, Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise.</p>								
						Total Periods	45	

REFERENCES:

1.	T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004 .
2.	B.Razavi, "RF Microelectronics", Pearson Education, 1997.
3.	Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.
4.	B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.



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Programme	M.E.	Programme Code	203	Regulation	2013
Department	APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE07	HARDWARE SOFTWARE CO-DESIGN	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To provide an in-depth knowledge of hardware software co-design. To provide the basics of hardware and software partitioning. To study the design of hardware software co synthesis. To study the design of prototyping and emulation. 							
Unit - I	SYSTEM SPECIFICATION AND MODELLING				Periods	9		
Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling Co-Design for Heterogeneous Implementation – Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification.								
Unit - II	HARDWARE/SOFTWARE PARTITIONING				Periods	9		
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation,Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem ,Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.								
Unit - III	HARDWARE/SOFTWARE CO-SYNTHESIS				Periods	9		
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.								
Unit - IV	PROTOTYPING AND EMULATION				Periods	9		
Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems.								
Unit - V	DESIGN SPECIFICATION AND VERIFICATION				Periods	9		
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co simulation.								

References:



1.	Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2.	Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.
3.	Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.

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Programme	M.E.	Programme Code		Regulation
Department	APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING			2013
				Semester

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE08	NANO ELECTRONICS	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To acquire knowledge about fundamental quantum mechanics. To study about architecture and operations of different nano structures. To comprehend the low dimension, high speed and low power design techniques and methodologies. 							
Unit - I	TECHNOLOGY AND ANALYSIS				Periods	9		
Film Deposition Methods – Lithography- Material removing techniques - Etching and Chemical-Mechanical Polishing - Scanning Probe Techniques.								
Unit - II	CARBON NANO STRUCTURES				Periods	9		
Carbon Clusters - Carbon Nano tubes – Fabrication – Electrical, Mechanical and Vibrational Properties – Applications of Carbon Nano tubes.								
Unit - III	LOGIC DEVICES				Periods	9		
Silicon MOSFET's – Novel materials and alternative concepts – Ferroelectric Field Effect Transistors – Super conductor digital electronics – Carbon Nano tubes for data processing.								
Unit - IV	RANDOM ACCESS MEMORIES AND MASS STORAGE DEVICES				Periods	9		
High Permittivity material for DRAM's – Ferro electric Random Access memories – Magneto- resistive RAM- Hard Disk Drives – Magneto Optical Disks – Rewriteable DVDs based on Phase Change Materials – Holographic Data Storage.								
Unit - V	DATA TRANSMISSION AND INTERFACES AND DISPLAYS				Periods	9		
Photonic Networks – Microwave Communication System – Liquid Crystal Displays – Organic Light emitting diodes.								
					Total periods	45		
REFERENCES:								
1.	Rainer Waser, Nano Electronics and Technology, Wiley VCH, 2003.							
2.	Charles Poole, Introduction to Nano Technology, Wiley Inter science, 2003.							



3.	C.Wasshuber, Simon , Simulation of Nano Structures Computational Single-Electronics, Springer-Verlag,2001.
4.	Rainer Waser, Nano Electronics and information technology advanced electronic materials and novel devices, Wiley –VcH Verlag GmbH-KgaH, Germany, 2005.
5.	A. Mark Reed and Takhee Lee, Molecular Nano Electronics, American Scientific Publisher, California,2003.
6.	Y.Takahashi. A Comparative Study of Single-Electron Memories, IEEE Trans. Electron Devices, 1998, pp.2365–2371.

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE05	ASIC DESIGN	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To study about ASIC fundamentals To study different level of ASIC flow in detail To explore modelling of ASIC design 		
Unit - I	INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN	Periods	9
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.			
Unit - II	PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS	Periods	9
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.			
Unit - III	PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY	Periods	9
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.			
Unit - IV	LOGIC SYNTHESIS, SIMULATION AND TESTING	Periods	9
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.			
Unit - V	ASIC CONSTRUCTION, FLOOR PLANNING,	Periods	9



PLACEMENT AND ROUTING		
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.		
Total Periods		45
REFERENCES:		
1.	M.J.S .Smith, " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.	
2.	Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991	
3.	S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.	
4.	Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.	
5.	S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.	
6.	Jose E. France, Yannis Tsividis,"Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.	

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Programme	M.E.	Programme Code		Regulation	2013
Department	APPLIED ELECTRONICS & VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P		C	CA	ESE
P13VD207	LOW POWER VLSI DESIGN	3	0	0	3	50	50	100

Objectives	<ul style="list-style-type: none"> To study the principle of low power design. To explore the concept of power optimization and estimation analysis. To understand the layout design and special techniques. To study the software design for low power techniques. 							
Unit - I	POWER DISSIPATION IN CMOS					Periods	9	
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.								
Unit - II	POWER OPTIMIZATION					Periods	9	
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.								
Unit - III	DESIGN OF LOW POWER CMOS CIRCUITS					Periods	9	
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.								
Unit - IV	POWER ESTIMATION					Periods	9	
Power estimation techniques – Logic level power estimation – Simulation power analysis– Probabilistic power analysis.								
Unit - V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER					Periods	9	
Synthesis for low power –Behavioral level transforms- Software design for low power								
						Total Periods	45	
REFERENCES:								
1.	K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000							
2.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002							
3.	J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.							
4.	A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.							
5.	Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.							



6.	Abdellatif Bellaouar, Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7.	James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD208	VLSI SIGNAL PROCESSING	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To study the DSP Systems, Pipelining and parallel processing of FIR Filters. To understand the concept of Retiming, Algorithmic strength reduction. To explore the Fast Convolution, Pipelining and Parallel Processing of IIR Filters. To understand Scaling, Round-Off Noise, Bit-Level Arithmetic Architectures and Numerical Strength Reduction, Synchronous, Wave And Asynchronous Pipelining. 		
Unit - I	INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS	Periods	9
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.			
Unit - II	RETIMING, ALGORITHMIC STRENGTH REDUCTION	Periods	9
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.			
Unit - III	FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS	Periods	9
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.			
Unit - IV	SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES	Periods	9
Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR			



filters.			
Unit - V	NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING	Periods	9
Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.			
		Total Periods	45
References:			
1.	Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and implementation “, Wiley, Interscience, 2007.		
2.	U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004.		

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester
				2013

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE02	ANALOG VLSI DESIGN	3	0	0	3	50	50	100



Objective	<ul style="list-style-type: none"> To study the basic CMOS & BICMOS circuit techniques in VLSI signal processing. To understand the concept of A/D Converters And Analog Integrated Sensors To Design For Testability And Analog VLSI Interconnects. To understand the concepts of Statistical Modeling and Simulation, Aided Design and Analog and Mixed Analog Digital Layout. 							
Unit - I	BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW- VOLTAGE SIGNAL PROCESSING				Periods	9		
Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filter.								
Unit - II	BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING				Periods	9		
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.								
Unit - III	SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS				Periods	9		
First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched- Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters- Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma- Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters- Sensors-Sensor Interfaces.								
Unit - IV	DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS				Periods	9		
Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam								

Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.			
Unit - V	STATISTICAL MODELING AND SIMULATION,ANALOG COMPUTER- AIDED DESIGN AND ANALOG AND MIXED ANALOG DIGITAL LAYOUT	Periods	9
Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.			
		Total Periods	45
REFERENCES:			
1.	Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw- Hill International Editons, 1994		
2.	Malcom R.Haskard, Lan C.May, "Analog VLSI Design - NMOS and CMOS ",PrenticeHall, 1998		
3.	Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990		
4.	Jose E.France, Yannis Tsvividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994		

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Department	VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD206	CAD FOR VLSI CIRCUITS	3	0	0	3	50	50	100



Objective	<ul style="list-style-type: none"> To provide an in-depth knowledge in VLSI Design methodology Enhance the fundamentals of different data structures To Analysis different types of floor planning, placement and routing algorithms. 							
Unit - I	VLSI DESIGN METHODOLOGIES					Periods	9	
Introduction to VLSI Design methodologies - Review of Data structures and algorithms -Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.								
Unit - II	DESIGN RULES					Periods	9	
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.								
Unit - III	FLOOR PLANNING					Periods	9	
Floor planning concepts - shape functions and Floor plan sizing - Types of local Routing problems - Area routing - channel routing - global routing - algorithms for global routing								
Unit - IV	SIMULATION					Periods	9	
Simulation - Gate-level modelling and simulation - Switch-level modelling and simulation- Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.								
Unit - V	MODELLING AND SYNTHESIS					Periods	9	
High level Synthesis - Hardware models - Internal representation - Allocation -assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.								
						Total Periods	45	
REFERENCES:								
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002							
FURTHER READINGS:								
1.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.							

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Department	APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE09	HIGH PERFORMANCE COMPUTER NETWORKS	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To develop a comprehensive understanding of network architectures, protocols, control, performances To focus on the convergence of computer networking, and wireless networks that explains current and emerging networking technologies. 							
Unit - I	INTRODUCTION					Periods	9	
Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing, SONET – DWDM–DSL–ISDN–BISDN, ATM.								
Unit - II	MULTIMEDIA NETWORKING APPLICATIONS					Periods	9	
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.								
Unit - III	ADVANCED NETWORKS CONCEPTS					Periods	9	
VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN. MPL Soperation, Routing, Tunneling and use of FEC, Traffic Engineering, and MPLS based VPN, overlay networks - P2P connections.								
Unit - IV	TRAFFIC MODELLING					Periods	9	
Little’s theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.								
Unit - V	NETWORK SECURITY AND MANAGEMENT					Periods	9	
Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls –attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1								
						Total Periods	45	
REFERENCES:								
1.	Walrand .J. Varatya, High performance communication network, Margan Kanffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.							
2.	J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet",							

	Pearson, 2nd edition, 2003.
3.	Nader F.Mir, Computer and Communication Networks, first edition.
FURTHER READINGS:	
5.	Aunurag kumar, D. MAnjunath, Joy kuri, “Communication Networking”, Morgan Kaufmann Publishers, 1ed 2004.
6.	Larry I.Peterson&Bruce S.David, “Computer Networks: A System Approach”-1996

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Programme	M.E.	Programme Code		Regulation
Department	COMPUTER SCIENCE, VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING			2013
				Semester

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE08	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3	50	50	100

Objective	<ul style="list-style-type: none"> To Understand Computer Design and Architecture To understand the state-of-the-art in parallel processing and computer hardware technologies 							
Unit – I	THEORY OF PARALLELISM				Periods	9		
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.								
Unit – II	PARTITIONING AND SCHEDULING				Periods	9		
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.								
Unit – III	HARDWARE TECHNOLOGIES				Periods	9		
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.								
Unit – IV	PIPELINING AND SUPERSCALAR TECHNOLOGIES				Periods	9		
Parallel and scalable architectures, Multiprocessor and Multicomputer, Multivectorand SIMD computers, Scalable, Multithreaded and data flow architectures.								
Unit – V	SOFTWARE AND PARALLEL PROGRAMMING				Periods	9		
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.								
					Total Periods	45		
REFERENCES:								
1.	Kai Hwang, “Advanced Computer Architecture ”, McGraw Hill International, 2001.							
FURTHER READINGS:								
1.	Dezso Sima, Terence Fountain, Peter Kacsuk, ”Advanced Computer architecture – A design							

	Space Approach” , Pearson Education , 2003.
2.	John P.Shen, “Modern processor design . Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
3.	John P.Shen, “Modern processor design . Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
4.	Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, Tata Mc-Graw Hill, 5th Edition, , 2002.