VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
(Autonomous Institution, Affiliated to Anna University, Chennai)
Elayampalayam, Tiruchengode – 637 205

M.E. APPLIED ELECTRONICS

Regulation 2015

CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEO_S)

PEO I. To acquire a background in Basic Science and Mathematics and ability to use these tools in Applied Electronics

PEO II. Teach students to understand the principles involved in the latest hardware and software required for designing and critically analyzing electronic circuits relevant to industry and society.

PEO III. Combine theory and laboratory to make students appreciate the concepts in the working of electronic circuits.

PEO IV. Mould students to be able to communicate efficiently

PEO V. Motivate students to take up socially relevant and challenging projects and propose innovative solution to problems for the benefit of society.

PROGRAMME OUTCOMES (PO_S)

PO 1. Apply knowledge of Mathematics, Science, Engineering fundamentals and an engineering specialization to the conceptualization of Engineering models.

PO 2. Identify, formulate, research literature and solve complex Electronics and Communication Engineering problems reaching substantiated conclusions using first principles of Mathematics and Engineering Sciences.

PO 3. Design solutions for complex Engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.

PO 4. Conduct investigations of complex problems including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.

PO 5. Create, select and apply appropriate techniques, resources, and modern Engineering tools, including prediction and modeling, to complex Electronics and Communication Engineering activities, with an understanding of the limitations.

PO 6. Function effectively as an individual, and as a member or leader in diverse teams and in multi - disciplinary settings.

PO 7. Communicate effectively on complex Electronics and Communication Engineering activities with the Engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 8. Demonstrate understanding of the societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to Engineering practice.

PO 9. Understand and commit to professional ethics and responsibilities and norms of Engineering practice.

PO 10. Understand the impact of Engineering solutions in a societal context and demonstrate knowledge of and need for sustainable development.

PO 11. Demonstrate a knowledge and understanding of management and business practices, such as risk and change management, and understand their limitations.

PO 12. Recognize the need for, and have the ability to engage in independent and lifelong learning.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES (PEO_S) WITH PROGRAMME OUTCOMES (PO_S)

A broad relation between the programme objective and the outcomes is given in the following table

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES											
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**
PEO 1	✓	✓					✓					
PEO 2			✓	✓	✓							✓
PEO 3				✓		✓						
PEO 4						✓				✓	✓	
PEO 5						✓	✓	✓	✓	✓	✓	✓

Sem	Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
I	Applied Mathematics	✓		✓		✓							
	Advanced Digital System Design	✓	✓	✓		✓							
	Solid State Devices	✓	✓										
	Advanced Digital Signal Processing	✓	✓	✓		✓							
	DSP Integrated Circuits	✓	✓	✓		✓							
	Professional Elective – I												
	Electronics Design Lab - I		✓		✓	✓						✓	
II	Analysis and Design of Analog Integrated Circuits	✓	✓	✓		✓							
	Digital Control Engineering	✓	✓	✓		✓	✓	✓	✓				
	Research Methodology and Data analysis				✓				✓				
	Professional Elective – II												
	Professional Elective – III												
	Open Elective – I												
	Electronics Design Lab – II		✓		✓	✓						✓	
	Technical Seminar				✓	✓	✓			✓	✓	✓	✓
III	Professional Elective – IV												
	Professional Elective - V												
	Open Elective - II												
	Project Phase – I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
IV	Project Phase – II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205					
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**	
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**	

CURRICULUM

(Applicable to the students admitted from the academic year 2015-2016 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
P15MA102	Applied Mathematics*	FC	3	0	0	3	50	50	100
P15AE101	Advanced Digital System Design *	PC	3	0	0	3	50	50	100
P15AE102	Solid State Devices*	PC	3	0	0	3	50	50	100
P15AE103	Advanced Digital Signal Processing	PC	3	0	0	3	50	50	100
P15AE104	DSP Integrated Circuits	PC	3	0	0	3	50	50	100
	Professional Elective – I	PE	3	0	0	3	50	50	100
PRACTICAL									
P15AE105	Electronics Design Lab - I	PC	0	0	4	2	50	50	100
					Total Credits	**20**	**350**	**350**	**700**

FC – Foundation Course
PC – Professional Core,
OE – Open Elective,
PE – Professional Elective,
EEC – Enhanced Employability Course,
CA - Continuous Assessment,
ESE - End Semester Examination

* Common Syllabus for M.E. VLSI Design

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205								
Programme	**M.E.**	Programme Code		**203**		Regulation		**2015**	
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**					Semester		**II**	
CURRICULUM (Applicable to the students admitted from the academic year 2015-2016 onwards)									
Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
P15AE206	Analysis and Design of Analog Integrated Circuits	PC	3	0	0	3	50	50	100
P15AE207	Digital Control Engineering	PC	3	0	0	3	50	50	100
P15AE208	Research Methodology and Data analysis *	EEC	3	0	0	3	50	50	100
	Open Elective – I	OE	3	0	0	3	50	50	100
	Professional Elective – II	PE	3	0	0	3	50	50	100
	Professional Elective – III	PE	3	0	0	3	50	50	100
PRACTICAL									
P15AE209	Electronics Design Lab – II	PC	0	0	4	2	50	50	100
P15AE210	Technical Seminar	EEC	0	0	2	1	100	-	100
					Total Credits	**21**	**450**	**350**	**800**

PC – Professional Core,
OE – Open Elective,
PE – Professional Elective,
EEC – Enhanced Employability Course,
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*Common syllabus for ME-CSE, ME- PSE, ME- VLSI Design & M. Tech- IT

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Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**	
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**III**	

CURRICULUM

(Applicable to the students admitted from the academic year 2015-2016 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
THEORY									
	Professional Elective – IV	OE	3	0	0	3	50	50	100
	Professional Elective - V	PE	3	0	0	3	50	50	100
	Open Elective - II	PE	3	0	0	3	50	50	100
PRACTICAL									
P15AE311	Project Phase – I	EEC	0	0	12	6	60	40	100
					Total Credits	**15**	**210**	**190**	**400**

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PE – Professional Elective,
EEC – Enhanced Employability Course,
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Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**	
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**IV**	

CURRICULUM

(Applicable to the students admitted from the academic year 2015-2016 onwards)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
PRACTICAL									
P15AE412	Project Phase – II	EEC	0	0	24	12	60	40	100
					Total Credits	**12**	**60**	**40**	**100**

EEC – Enhanced Employability Course,
CA - Continuous Assessment,
ESE - End Semester Examination

Cumulative Course Credits - 68

PROFESSIONAL CORE (PC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P15AE101	Advanced Digital System Design	PC	3	0	0	3	50	50	100
P15AE102	Solid State Devices	PC	3	0	0	3	50	50	100
P15AE103	Advanced Digital Signal Processing	PC	3	0	0	3	50	50	100
P15AE104	DSP Integrated Circuits	PC	3	0	0	3	50	50	100
P15AE105	Electronics Design Lab - I	PC	0	0	4	2	50	50	100
P15AE206	Analysis and Design of Analog Integrated Circuits	PC	3	0	0	3	50	50	100
P15AE207	Digital Control Engineering	PC	3	0	0	3	50	50	100
P15AE209	Electronics Design Lab – II	PC	0	0	4	2	50	50	100

ENHANCED EMPLOYABILITY COURSES (EEC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P15AE208	Research Methodology and Data analysis	EEC	3	0	0	3	50	50	100
P15AE210	Technical Seminar	EEC	0	0	2	1	100	-	100
P15AE412	Project Phase – II	EEC	0	0	24	12	50	50	100

FOUNDATION COURSE (FC)

Course Code	Course Name	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CA	ESE	Total
P15MA102	Applied Mathematics*	FC	3	0	0	3	50	50	100

PROFESSIONAL ELECTIVE (PE)

Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE01	Digital Image Processing	3	0	0	3	50	50	100
P15AEE02	VLSI Design	3	0	0	3	50	50	100
P15AEE03	Hardware Software Co-Design	3	0	0	3	50	50	100
P15AEE04	Advanced Processors	3	0	0	3	50	50	100
P15AEE05	Electromagnetic Interference and Compatibility in System Design	3	0	0	3	50	50	100
P15AEE06	Low Power VLSI Design	3	0	0	3	50	50	100
P15AEE07	High Performance Computer Networks	3	0	0	3	50	50	100
P15AEE08	Embedded System Design	3	0	0	3	50	50	100
P15AEE09	RF Microelectronic chip design	3	0	0	3	50	50	100
P15AEE10	CMOS Analog VLSI Design	3	0	0	3	50	50	100
P15AEE11	Reliability Engineering	3	0	0	3	50	50	100
P15AEE12	VLSI Signal Processing	3	0	0	3	50	50	100
P15AEE13	ASIC Design	3	0	0	3	50	50	100
P15AEE14	Foundations of VLSI CAD	3	0	0	3	50	50	100
P15AEE15	Power Electronics	3	0	0	3	50	50	100
P15AEE16	Computer Architecture and Parallel Processing	3	0	0	3	50	50	100
P15AEE17	Pattern Recognition and Artificial Intelligence	3	0	0	3	50	50	100
P15AEE18	Soft Computing	3	0	0	3	50	50	100
P15AEE19	Neural Networks and its Applications	3	0	0	3	50	50	100

P15AEE20	Nano Electronics	3	0	0	3	50	50	100
P15AEE21	System Design using FPGA	3	0	0	3	50	50	100
P15AEE22	DSP Processor Architecture and Programming	3	0	0	3	50	50	100
P15AEE23	Embedded Systems in Automotive Applications	3	0	0	3	50	50	100
P15AEE24	Medical Image Processing	3	0	0	3	50	50	100
P15AEE25	Robotics	3	0	0	3	50	50	100

CA - Continuous Assessment,

ESE - End Semester Examination

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Programme	**M.E.**	Programme Code	**203**		Regulation		**2015**	
Department	**VLSI DESIGN & APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		**I**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15MA102	**Applied Mathematics**	3	0	0	3	50	50	100
Course Objective	• To expose fundamental knowledge in 1D Random Variables and testing the hypothesis. • To analyze linear programming, Computational methods in Engineering and various queuing models.							
Unit – I	**ONE DIMENSIONAL RANDOM VARIABLE**					Periods	**9**	
Random Variables- Probability Function-Moments-Moment Generating Function & their Properties- Binomial, Poisson, Geometric, Uniform, Exponential Distributions.								
Unit – II	**TESTING OF HYPOTHESIS**					Periods	**9**	
Basiic Definitions:- (Population, Sampling, Tests of Significance, Testing a Hypothesis, Null Hypothesis, Alternative Hypothesis, Level of Significance, Types of Errors) – Testing of Hypothesis using : 't'-Test , 'F'-Test , Chi Square Test (ψ^2) - Test for Independence of Attributes & Goodness of Fit.								
Unit – III	**LINEAR PROGRAMMING**					Periods	**9**	
Formulation-Graphical solution-Simplex Method -Transportation and Assignment problems.								
Unit – IV	**DYNAMIC PROGRAMMING**					Periods	**9**	
Dynamic Programming-principle of optimality-forward and backward recursion-DP Applications (Cargo loading method)-Problems of dimensionality.								
Unit – V	**QUEUING MODELS**					Periods	**9**	
Introduction-Markovian Models: M/M/1**:** infinite capacity-M/M/C**:** infinite capacity-M/M/1**:** finite capacity – M/M/C **:** finite capacity, Little's formula.								
						Total Periods	**60**	

REFERENCES:

1.	B.V.Ramana – 'Higher Engineering Mathematics', by Tata Mc Graw Hill Publishing Pvt Ltd – New Delhi, 2008 Edition.
2.	Taha,H.a., Operations Research: An Introduction,seventh Edition,Person Education edition,Asia,New Delhi(2002).
3.	Moon,T.K.,Sterling,W.C.,Mathematical methods and algorithms for signal processing,Pearson Education,2000
4.	Donald Gross and carl M.Harris, Fundamentals of queuing theory,2nd edition, john Wiley and Sons,New York(1985)
5.	Richard Johnson,Miller&freund's probability and statistics for engineers,7th edition, Prentice-Hall of india,private Ltd.,New Delhi(2007)

Course Outcome	• Can expose fundamental knowledge in 1D Random Variables and testing the hypothesis. • Able to analyze linear programming, Computational methods in Engineering and various queuing models.

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Department	**VLSI DESIGN & APPLIED ELECTRONICS /ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	**I**		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE101	**Advanced Digital System Design**	3	0	0	3	50	50	100
Course objective	• To provide an in-depth knowledge of synchronous and asynchronous sequential circuits analysis and design. • To provide the basics of fault diagnosis and testing algorithms. • To study the design of synchronous sequential circuits using PLDs. • To study the design of digital systems using VHDL.							
Unit - I	**SEQUENTIAL CIRCUIT DESIGN**					Periods		**9**
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits -design of iterative circuits-ASM chart and realization using ASM.								
Unit - II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**					Periods		**9**
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.								
Unit - III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**					Periods		**9**
Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.								
Unit - IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**					Periods		**9**
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.								
Unit - V	**SYSTEM DESIGN USING VHDL**					Periods		**9**
VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier-Divider – Design of simple microprocessor.								
						Total Periods		**45**

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004

FURTHER READINGS:

1. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
2. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
3. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
4. Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004
5. Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill – 2006

Course	• Provides an in-depth knowledge of synchronous and asynchronous sequential circuits

Outcome	analysis and design. • Provides the basics of fault diagnosis and testing algorithms. • Able to study the design of synchronous sequential circuits using PLDs. • Able to study the design of digital systems using VHDL.

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Programme	**M.E.**	Programme code	**203**	Regulation	**2015**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE102	**Solid State Devices**	3	0	0	3	50	50	100

Course Objective

- To study and model MOSFET and advanced MOSFET.
- To Model the Process Variation and quality assurance.
- To study the opto electronic devices.
- To understand the concepts of high frequency and high power devices.

Unit- I	**MOSFET DEVICE PHYSICS**	Periods	**9**

Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

Unit- II	**METAL OXIDE SEMICONDUCTOR FET**	Periods	**9**

High Electron Mobility Transistor - Short channel Effects – Metal Insulator Semiconductor FET - Basic Operation and Fabrication - Effects of Real Surfaces - Threshold Voltage - MOS capacitance Measurements - current – Voltage Characteristics of MOS Gate Oxides - MOS Field Effect Transistor – Output Characteristics - Transfer characteristics - Short channel MOSFET V-I characteristics -Control of Threshold Voltage - Substrate Bias Effects - Sub threshold characteristics -Equivalent Circuit for MOSFET - MOSFET Scaling and Hot Electron Effects - Drain -Induced Barrier Lowering - short channel and Narrow Width Effect - Gate Induced Drain Leakage.

Unit- III	**OPTO ELCTRONIC DEVICES**	Periods	**9**

Photodiodes - Current and Voltage in illuminated Junction - Solar Cells - Photo detectors- Noise and Bandwidth of Photo detectors - Light Emitting Diodes - Light Emitting Materials - Fiber Optic Communications Multilayer Hetero junctions for LEDs - Lasers -Semiconductor lasers - Population Inversion at a Junction Emission Spectra for p-n junction - Basic Semiconductor lasers - Materials for Semiconductor lasers.

Unit- IV	**ENERGY BANDS AND CHARGE CARRIERS IN SEMICONDUCTORS AND JUNCTIONS**	Periods	**9**

Energy bands in Solids, Energy Bands in Metals, Semiconductors, and Insulators -Direct and Indirect Semiconductors-Charge Carriers in Semiconductors - Electrons and Holes - Electrons and Holes in Quantum Wells - Carrier Concentrations - Fermi Level - Electron and Hole Concentrations at Equilibrium - Temperature Dependence of Carrier Concentrations -Compensation and Space Charge Neutrality - Drift of Carrier in Electric and Magnetic Fields conductivity and Mobility - Drift and Resistance - Effects of Temperature and Doping on Mobility - High field effects - Hall Effect - invariance of Fermi level at equilibrium - Fabrication of p-n junctions, Metal semiconductor junctions.

Unit- V	**HIGH FREQUENCY AND HIGH POWER DEVICES**	Periods	**9**

Tunnel Diodes, IMPATT Diode, operation of TRAPATT and BARITT Diodes, Gunn Diode - transferred - electron mechanism, formation and drift of space charge domains-n-p-n Diode, Semiconductor Controlled Rectifier, Insulated Gate Bipolar Transistor.

Total Periods	**45**

REFERENCES:

1.	Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003.
2.	Christian C. Enz, Eric A. Vittoz, "Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design", John Wiley & Sons, Ltd, 2006.
3.	Donald A. Neaman, Semiconductor Physics and Devices, 3rd Edition, TMH, 2002.
4.	Yannis Tsividis, Operation & Mode line of MOS Transistor, 2nd Edition, Oxford University Press, 1999.
5.	Nandita Das Gupta & Aamitava Das Gupta, Semiconductor Devices Modeling a Technology, PHI, 2004.
6.	D.K. Bhattacharya & Rajinish Sharma, Solid State Electronic Devices, Oxford University Press, 2007.
Course Outcome	• Able to study and model MOSFET and advanced MOSFET. • Can be Modeled the Process Variation and quality assurance. • Design and analysis of various types of diodes. • Identification of new developments in solid state devices.

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Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION**			Semester	**I**			

Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE103	**Advanced Digital Signal Processing**	3	0	0	3	50	50	100

Course Objective	• To study the multirate FIR filter design. • To explore the concepts of multi rate signal processing and multi rate filters. • To study the adaptive filters and its applications. • To learn fundamental concepts on signal processing in power spectrum estimation.

Unit – I	**MULTIRATE SIGNAL PROCESSING**	Periods	**9**

Introduction-Sampling and Signal Reconstruction-Sampling rate conversion – Decimation by an integer factor – interpolation by an integer factor –Sampling rate conversion by a rational factor –poly-phase FIR structures – FIR structures with time varying coefficients - Sampling rate conversion by a rational factor-Multistage design of decimator and interpolator.

Unit – II	**MULTIRATE FIR FILTER DESIGN**	Periods	**9**

Design of FIR filters for sampling rate conversion –Applications of Interpolation and decimation in signal processing –Filter bank implementation –Two channel filter banks-QMF filter banks –Perfect Reconstruction Filter banks – tree structured filter banks - DFT filter Banks – M-channel filter banks- octave filter banks

Unit – III	**ADAPTIVE FILTERS**	Periods	**9**

FIR Adaptive filters - Newton's steepest descent method – Adaptive filters based on steepest descent method - LMS Adaptive algorithm – other LMS based adaptive filters- RLS Adaptive filters - Exponentially weighted RLS - Sliding window RLS - Simplified IIR LMS Adaptive filter-Applications: Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation.

Unit – IV	**POWER SPECTRAL ESTIMATION**	Periods	**9**

Estimation of spectra from finite duration observations of a signal –The Periodogram-Use of DFT in Power spectral Estimation –Non-Parametric methods for Power spectrum Estimation – Bartlett. Welch and Blackman–Tukey methods –Comparison of performance of Non – Parametric power spectrum Estimation methods – Application: speech enhancement using power spectrum estimation

Unit – V	**PARAMETRIC METHODS OF POWER SPECTRUM ESTIMATION**	Periods	**9**

Relationship between auto correlation and model parameters – AR (Auto –Regressive) process and Linear prediction –Yule –Walker, Burg & Unconstrained Least squares methods –Moving average (MA) and ARMA Models – Minimum variance method –Pisarenko's harmonic De composition Method – MUSIC method.

Total Periods	**45**

REFERENCES:

1.	H. Monson Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc., 2008.
2.	G.. John Proakis and G. Dimitris Manolakis, Digital Signal Processing, Pearson Education, 2006.
3.	P.P.Vaidyanathan , Multirate Syatems and Filter Banks, Pearson Education, 2008
4.	N.J.Filege, Multirate Digital Signal Processing, John Wiley and Sons, 2000.
5.	G..John Proakis, Algorithms for Statistical Signal Processing, Pearson Education, 2002.
6.	G.Dimitris and G.Manolakis., Statistical and Adaptive Signal Processing, McGraw Hill, 2002
7.	Sophoncles J. Orfanidis, Optimum Signal Processing, McGraw Hill, 2007.

Course Outcome	• Acquiring knowledge of how a multi rate system works. • Ability to design and implement decimator and interpolator and to design multi rate

	filter bank. • Understanding different spectral estimation techniques and linear prediction. • Ability to design LMS and RLS adaptive filters for signal enhancement, channel equalization.

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Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**			
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE104	**DSP Integrated Circuits**	3	0	0	3	50	50	100
Course Objective	• To study the advanced digital signal processors and IC technologies. • To explore the concepts of multi rate signal processing and multi rate filters. • To study the complex multipliers and VLSI layouts. • To understand the concept of layout of VLSI circuits .							
Unit – I	**DSP INTEGARTED CIRCUITS & VLSI CIRCUIT TECHNOLOGIES**				Periods	**9**		
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.								
Unit – II	**DIGITAL SIGNAL PROCESSING**				Periods	**9**		
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.								
Unit – III	**DIGITAL FILTERS AND FINITE WORD LENGTH**				Periods	**9**		
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.								
Unit – IV	**DSP ARCHITECTURES & SYNTHESIS OF DSP ARCHITECTURES**				Periods	**9**		
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputer, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.								
Unit – V	**SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS**				Periods	**9**		
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. CORDIC algorithm.								
					Total Periods	**45**		
REFERENCES:								
1.	Lars Wan hammer, "DSP Integrated Circuits", Academic press, New York 1999							
2.	Oppenheim A.V. et.al, 'Discrete-time Signal Processing' Pearson education,2000							
FURTHER READINGS:								

1.	Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second edition, Pearson education, Asia 2001 practical approach", Second edition, Pearson education, Asia 2001
2.	Keshab K.Parhi, 'VLSI digital Signal Processing Systems design and Implementation' John Wiley & Sons, 1999
Course Outcome	• Able to study the advanced digital signal processors and IC technologies. • Able to explore the concepts of multi rate signal processing and multi rate filters. • Can be analyzing the complex multipliers and VLSI layouts. • Able to analyze the synchronous and asynchronous sequential circuits

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**			

Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE105	**Electronic Design Lab – I**	0	0	4	2	50	50	100

Course Objective	• To design and implement a system using microprocessor and microcontrollers • To model and simulate sequential systems using HDL • To Design and implement circuits in FPGA. • To Design and implement circuits using SPICE.

Suggested list of experiments:

1.	System design using PIC Microcontroller.
2.	Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor
3.	Simulation of QMF using Simulation Packages
4.	Modeling of Sequential Digital system using VHDL.
5.	Modeling of Sequential Digital system using Verilog.
6.	Design and Implementation of ALU using FPGA
7.	Simulation of NMOS and CMOS circuits using SPICE.
8.	System design using 16- bit Microprocessor.

TOTAL PERIODS: 60 Hours

Course Outcome	• Design and implementation of a system using microprocessor and microcontrollers • Modeling and simulation of a sequential systems using HDL(s) • Design and implementation of circuits in FPGA. • Analyze NMOS and CMOS circuits using SPICE.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**			
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE206	**Analysis and Design of Analog Integrated Circuits**	3	0	0	3	50	50	100
Course Objective	• To provide an in-depth knowledge in computer fundamentals. • To provide the basics of C programming language. • To enhance the fundamental Application relevant to C programming language. • To study the concept of operational amplifiers.							
Unit – I	**MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES**				Periods	**9**		
Depletion region of PN junction– Large signal behavior of Bipolar Transistors–small signal model of bipolar transistors – large signal behavior of MOSFET – small signal of MOS transistors – short channel effects in MOS transistors– Weak inversion in MOS transistors – substrate current flow in MOS transistor.								
Unit – II	**CIRCUIT CONFIGURATION FOR LINEAR IC**				Periods	**9**		
Current sources, Analysis of differential amplifiers with active load using BJT and FET, supply and temperature independent biasing technique, voltage references, output stages: current follower, source follower and push pull output stages.								
Unit – III	**OPERATIONAL AMPLIFIERS**				Periods	**9**		
Analysis of operational amplifier circuit, slew rate model and high frequency analysis, frequency response of integrated circuits: single stage and multistage amplifier and operational amplifiers noise.								
Unit – IV	**ANALOG MULTIPLIER AND PLL**				Periods	**9**		
Analysis of four quadrants and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL-monolithic PLL design in integrated circuits: Sources of noise-noise model of integrated circuit components-circuit noise calculations-equivalent noise input generators-noise bandwidth-noise figure and noise temperature.								
Unit – V	**ANALOG DESIGN WITH MOS TECHNOLOGY**				Periods	**9**		
MOS current mirrors-simple, cascade, Wilson and widlar current sources-CMOS class AB output stages-two stage MOS operational amplifiers, with cascade, telescopic-cascade operational amplifiers-MOS folded cascade and MOS active cascade operational amplifiers.								
					Total Periods	**45**		
REFERENCES:								
1.	Gray, Meyer, Lewis and Hurst, "Analysis and design of analog ICs",Fourth Edition, Willey International,2002							
2.	Behzad Razavi,"Principles of data conversion system design",S.Chand and company ltd,2000							
FURTHER READINGS:								
1.	Nandita Dasgupta,Amitava Dasgupta,"Semiconductor devices ,modeling and technology",Prentice Hall of India Pvt Ltd,2004							
2.	Grebene,Bipolar and MOS Analog Integrated ciruit design", John Wiley and sons.Inc.2003							
3.	Phillip.E.Allen Douglas R Holberg ,CMOS Analog Integrated circuit design", second edition – Oxford University Press.2003							

Course Outcome	• Provides an in-depth knowledge in computer fundamentals. • Provides the basics of C programming language. • Enhance the fundamental Application relevant to C programming language. • Explain PLL types and analog multiplier

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS /ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	**II**		
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE207	**Digital Control Engineering**	3	0	0	3	50	50	100

Course Objective	• To understand different types of controllers. • To enhance the sampling techniques. • To design different digital control algorithms. • To understand the concept of digital control algorithms.

Unit – I	**PRINCIPLES OF CONTROLLERS**	Periods	**9**

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

Unit – II	**SIGNAL PROCESSING IN DIGITAL CONTROL**	Periods	**9**

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

Unit – III	**MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM**	Periods	**9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

Unit – IV	**DESIGN OF DIGITAL CONTROL ALGORITHMS**	Periods	**9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

Unit – V	**PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS**	Periods	**9**

Algorithm development of PID control algorithms, software implementation, Implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

	Total Periods **45**

REFERENCES:

1.	M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, NewDelhi, 1997.
2.	John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3.	Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

Course Outcome	• Able to understand different types of controllers. • Enhance the sampling techniques. • Able to Design PI, PD, PID controllers. • Analyze the concept of mathematical model of sample and hold.

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Programme	**M.E.**	Programme code	**203**		Regulation	**2015**		
Department	**ME-CSE, ME- PSE, ME- VLSI, ME- AE & M. Tech- IT**				Semester	**II**		
Course code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE208	**Research Methodology and Data Analysis**	3	0	0	3	50	50	100
Course Objective	• To understand the importance of Research • To acquire knowledge in Data Collection and Analysis of Data • To effectively write reports							
Unit - I	**INTRODUCTION TO RESEARCH**				Periods	**7**		
Nature, scope, and design of social research; Review of literature: qualitative (literary), quantitative (meta-analysis)								
Unit - II	**HYPOTHESIS**				Periods	**9**		
Hypothesis: sources, types and characteristics; Sample survey: sample and census survey, probability, non-probability and mixed sampling;								
Unit - III	**DATA COLLECTION**				Periods	**11**		
Methods of data collection: historical method, case study, observation, ethnographic methods, interview, questionnaire, focus group discussion, participatory rural appraisal, experimental method, pre-testing, and pilot survey; Scaling techniques different scales, item analysis, reliability, validity; Method of secondary data collection: sources, sample criteria, characteristics;								
Unit - IV	**DATA ANALYSIS**				Periods	**9**		
Data analysis: descriptive statistics, mean difference test, analysis of variance and experimental design; Bivariate and multivariate correlation and regression; Factor analysis, Cluster analysis, Discriminant analysis, Structural equation modelling, non-parametric statistics, Content analysis								
Unit - V	**REPORT WRITING**				Periods	**9**		
Report writing: review, qualitative, and empirical article writing.								
					Total Periods	**45**		
REFERENCES:								
1.	C.M.Chaudhary, "Research Methodology", RBSA Publishers, Jaipur, India 2009.							
2.	R.Paneerselvam, "Research Methodology", PHI Learning Pvt Ltd.,New Delhi 2009.							
Course Outcome	• Can formulate researchable questions • Can define a research strategy and design a research project to answer a research question • Can discuss the practice and principles of qualitative and quantitative social research							

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	**II**		
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AE209	**Electronics Design Lab - II**	0	0	4	2	50	50	100
Course Objective	• To illustrate the design, application, and limitations of electronic circuits by laboratory experience. • To able to design and simulate the digital control system using MATLAB tools. • To design PLL and CPLD • To design elevator controller using microcontroller.							
Suggested list of experiments:								
1. System design using PLL.								
2. System design using CPLD.								
3. Alarm clock using embedded micro controller.								
4. Model train controller using embedded micro controller.								
5. Elevator controller using embedded micro controller.								
6. Simulation of Non adaptive Digital Control System using MAT LAB control system Toolbox.								
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.								
TOTAL: 60 HOURS								
Course Outcome	• Able to illustrate the design, application, and limitations of electronic circuits by laboratory experience. • Able to design and simulate the digital control system using MATLAB tools. • Able to design PLL and CPLD circuits using microcontroller. • Able to design elevator controller using microcontroller.							

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	**-**		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE01	**Digital Image Processing**	3	0	0	3	50	50	100
Course objective	• To study about the digital image representation • To understand image representation and transformation techniques. • To learn about image segmentation and shape representation schemes. • To understand the morphological concepts in segmentation • To study about object recognition and image data compression.							
Unit - I	**IMAGE REPRESENTATION AND BACKGROUND**				Periods	**9**		
Image representation, Image digitization, Digital image properties. Color images and Cameras: an overview. Mathematical and physical background: Linear integral transforms, Image as stochastic processes.								
Unit - II	**DATA STRUCTURES AND IMAGE PRE-PROCESSING**				Periods	**9**		
Levels of image data representation, traditional image data structures, hierarchical data structures. Image Pre-Processing: Pixel brightness transformations, geometric transformations, local preprocessing and image restoration.								
Unit – III	**IMAGE SEGMENTATION AND SHAPE REPRESENTATION**				Periods	**9**		
Thresholding, Edge based and region based segmentation, active contour models and geometric deformable models. Contour based shape representation and description.								
Unit – IV	**MATHEMATICAL MORPHOLOGY**				Periods	**9**		
Morphological concepts, principles, binary dilation and erosion, gray scale dilation and erosion, skeletons and object marking, morphological segmentation and watersheds.								
Unit – V	**OBJECT RECOGNITION AND IMAGE DATA COMPRESSION**				Periods	**9**		
Knowledge representation, statistical pattern recognition, Neural nets. Image compression: Discrete time transforms in image compression, predictive compression methods, vector quantization, Hierarchical and progressive compression methods, coding and JPEG & MPEG compression.								
					Total periods	**45**		
REFERENCES:								
1.	Milan Sonka, Vaclav Hlavac, Roger Boyle, “Digital Image Processing and Computer Vision”, Cengage Learning, 2008.							
2.	S.Jayaraman, S.Esakkirajan and T.Veerakumar, “Digital Image Processing”, TMH Education Pvt. Ltd, New Delhi, 2009.							
3.	Rafael C. Gonzalez, Richard E. Woods, Steven L. Eddins, “Digital Image Processing using MATLAB”, Pearson Education, 2006.							
4.	Anil K- Jain- ‘Fundamentals of Digital Image Processing’- Pearson/Prentice Hall of India- 2002							
Course Outcome	• Study about the digital image representation • Understand image representation and transformation techniques.							

	• Learn about image segmentation and shape representation schemes. • Understand the morphological concepts in segmentation

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Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**-**			

Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE02	**VLSI Design**	3	0	0	3	50	50	100

Course Objective

- To understand the concepts of NMOS and PMOS transistors.
- To understand the Basic CMOS technology.
- To study the Multiplexers.
- To understand the concepts of digital design with Verilog HDL.

Unit – I	**MOS TRANSISTOR THEORY**	Periods	**9**

NMOS Enhancement Transistor and PMOS Enhancement transistors, Threshold voltage- Body effect- MOS device design equations-MOS Models-Small signal AC characteristics-Complementary CMOS Inverter-DC Characteristics-Static Load MOS Inverters.

Unit – II	**CMOS PROCESSING TECHNOLOGY AND LOGIC DESIGN**	Periods	**9**

Silicon Semiconductor Technology- overview- Basic CMOS technology-CMOS process Enhancements: Interconnect –Circuit Elements-Layout Design Rules-Latch UP- Switch Logic-Design of ALU subsystem-Design of Manchester Carry Chain.

Unit – III	**CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION**	Periods	**9**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, CMOS –Gate transistor sizing, power dissipation and design margining, Charge sharing ,Yield and Reliability-Scaling of MOS transistor.

Unit – IV	**SUBSYSTEM DESIGN AND LAYOUT**	Periods	**9**

Gate logic-Combinational Logic-Clocked Sequential Circuits-Precharged Bus Concept-Power dissipation for CMOS and BICMOS circuits-Design of 4-bit arithmetic Processor-Design of 4-bit Shifter-Memory elements-Finite State Machines.

Unit – V	**VERILOG HARDWARE DESCRIPTION LANGUAGE**	Periods	**9**

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

	Total Periods	**45**

REFERENCES:

1.	N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985
2.	Douglas.A.Pucknell Kamran Eshranghian,"Basic VLSI Design", 3rd Edition, 1994.
3.	Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4.	Eugene D.Fabricius, Introduction to VLSI Design, McGraw Hill International Editions, 1990.

Course Outcome

Able to

- Understand the concepts of NMOS and PMOS transistors.
- Understand the Basic CMOS technology.
- Analyze power dissipation in CMOS and BICMOS.
- Understand the concepts of digital design with Verilog HDL.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	-		
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE03	**Hardware Software Co-design**	3	0	0	3	50	50	100
Course Objective	• To provide an in-depth knowledge of hardware software co-design. • To provide the basics of hardware and software partitioning. • To provide information on current Hardware/Software Design Process. • To study the design of hardware software co synthesis. • To study the design of prototyping and emulation.							
Unit - I	**SYSTEM SPECIFICATION AND MODELLING**				**Periods**	**9**		
Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modeling Co-Design for Heterogeneous Implementation – Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification.								
Unit - II	**HARDWARE/SOFTWARE PARTITIONING**				**Periods**	**9**		
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, and HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.								
Unit - III	**HARDWARE/SOFTWARE CO-SYNTHESIS**				**Periods**	**9**		
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.								
Unit - IV	**PROTOTYPING AND EMULATION**				**Periods**	**9**		
Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future, Developments in Emulation and Prototyping, Target Architecture - Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.								
Unit - V	**DESIGN SPECIFICATION AND VERIFICATION**				**Periods**	**9**		
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co simulation.								
REFERENCES:								
1.	Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.							
2.	Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.							

3.	Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design "Kaufmann Publishers, 2001.
Course Outcome	The student will be able to • Analyze the Single-Processor Architectures • Understand the concepts of prototyping and emulation. • Analyze the Design Representation for System Level Synthesis • Analyze the Hardware/Software Co-Synthesis

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Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	-		
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE04	**Advanced Processors**	3	0	0	3	50	50	100

Course Objective	• To instruct information about the microprocessor architecture • To study the fundamentals of CISC architecture – Pentium • To impart knowledge on the operation of special purpose processors • To study ARM920T and ARM940T.

Unit - I	**MICROPROCESSOR ARCHITECTURE**	**Periods**	**9**
Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set Computer principles – RISC versus CISC – RISC properties – RISC evaluation.			
Unit - II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM**	**Periods**	**9**
The software model – functional description – CPU pin descriptions – Addressing modes –Processor flags – Instruction set – Bus operations – Super scalar architecture – Pipe lining – Branch prediction – The instruction and caches – Floating point unit– Programming the Pentium processor			
Unit - III	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM INTERFACE**	**Periods**	**9**
Protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts - Input /Output – Virtual 8086 model – Interrupt processing.			
Unit - IV	**HIGH PERFORMANCE RISC ARCHITECTURE: ARM**	**Periods**	**9**
ARM architecture – ARM assembly language program: Data processing instructions, Data Transfer instructions, Control flow instructions- ARM organization and implementation:3-Stage Pipeline ARM organization,5-Stage pipeline organization, ARM instruction execution, ARM implementation- ARM instruction set.			
Unit - V	**ARM PROCESSOR CORES AND ITS APPLICATIONS**	**Periods**	**9**
Thumb instruction set-ARM7TDMI, ARM8, ARM9TDMI, The ARM810, Strong ARMSA-10, ARM920T and ARM940T, The ARM1020E, VLSI Ruby II Advanced Communication Processor, VLSI ISDN Subscriber Processor, Ericsson-VLSI Bluetooth Baseband Controller.			

REFERENCES:

1	Daniel Tabak, "Advanced Microprocessors", McGraw Hill.Inc., 1995
2	James L. Antonakos, "The Pentium Microprocessor", Pearson Education, 1997.
3.	Steve Furber, "ARM System –On –Chip architecture", Addison Wesley, 2000.

Course Outcome	• Able to instruct information about the microprocessor architecture • Able to study the fundamentals of CISC architecture – Pentium • Able to impart knowledge on the operation of special purpose processors • Able to analyze high performance RISC architecture in ARM.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	**-**		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE05	**Electromagnetic Interference and Compatibility in System Design**	3	0	0	3	50	50	100

Course Objective	• To study the Electromagnetic Interference concepts, coupling principles and Control Techniques. • To design PCB for Electromagnetic compatibility. • To study instruments and measurements for Electromagnetic Interference. • To study EMI measurements and standards.

Unit - I	**EMI/EMC CONCEPTS**	Periods	**9**
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.			
Unit - II	**EMI COUPLING PRINCIPLES**	Periods	**9**
Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.			
Unit - III	**EMI CONTROL TECHNIQUES**	Periods	**9**
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.			
Unit - IV	**EMC DESIGN OF PCBS**	Periods	**9**
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.			
Unit - V	**EMI MEASUREMENTS AND STANDARDS**	Periods	**9**
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.			
		Total Periods	**45**

REFERENCES:

1.	V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2.	Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3.	Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.
4.	C.R.Paul,”Introduction to Electromagnetic Compatibility”, John Wiley and Sons, Inc, 1992.
5.	Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

Course Outcome	• Able to study the Electromagnetic Interference concepts, coupling principles and Control Techniques. • Able to design PCB for Electromagnetic compatibility. • Able to study instruments and measurements for Electromagnetic Interference. • Demonstrate the concepts of EMC design of PCBS

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE06	**Low Power VLSI Design**	3	0	0	3	50	50	100

Course Objective	• To study the principle of low power design. • To explore the concept of power optimization and estimation analysis. • To understand the layout design and special techniques. • To study the software design for low power techniques.

Unit - I	**POWER DISSIPATION IN CMOS**	Periods	**9**
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.			
Unit - II	**POWER OPTIMIZATION**	Periods	**9**
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.			
Unit - III	**DESIGN OF LOW POWER CMOS CIRCUITS**	Periods	**9**
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.			
Unit - IV	**POWER ESTIMATION**	Periods	**9**
Power estimation techniques – Logic level power estimation – Simulation power analysis– Probabilistic power analysis.			
Unit - V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER**	Periods	**9**
Synthesis for low power –Behavioral level transforms- Software design for low power			
		Total Periods	**45**

REFERENCES:

1.	K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002
3.	J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4.	A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5.	Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6.	Abdellatif Bellaouar, Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7.	James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

Course Outcome	• An ability to analyze different source of power dissipation and the factors involved in. • Able to understand the different techniques involved in low power adders and multipliers • An ability to identify and analyze the different techniques involved in reducing power consumption in adders and multipliers • Able to understand various power estimation techniques.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE07	**High Performance Computer Networks**	3	0	0	3	50	50	100
Course Objective	• To develop a comprehensive understanding of network architectures, protocols, control, performances. • To focus on the convergence of computer networking, and wireless networks that explains current and emerging networking technologies. • To study traffic modeling. • To understand the concept of network security and management.							
Unit - I	**INTRODUCTION**				Periods	**9**		
Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing.SONET – DWDM–DSL–ISDN–BISDN, ATM.								
Unit - II	**MULTIMEDIA NETWORKING APPLICATIONS**				Periods	**9**		
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.								
Unit - III	**ADVANCED NETWORKS CONCEPTS**				Periods	**9**		
VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN. MPL Soperation, Routing, Tunneling and use of FEC, Traffic Engineering, and MPLS based VPN, overlay networks - P2P connections.								
Unit - IV	**TRAFFIC MODELLING**				Periods	**9**		
Little's theorem, Need for modeling, Poisson modeling and its failure, Non- Poisson models, Network performance evaluation.								
Unit - V	**NETWORK SECURITY AND MANAGEMENT**				Periods	**9**		
Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls –attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1								
					Total Periods	**45**		

REFERENCES:

1.	Walrand .J. Varatya, High performance communication network, Margan Kanffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.
2.	J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
3.	Nader F.Mir, Computer and Communication Networks, first edition.

FURTHER READINGS:

1.	Aunurag kumar, D. MAnjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.
2.	LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
3.	Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson

	education 2003.
4.	Larry l.Peterson&Bruce S.David, “Computer Networks: A System Approach”-1996
Course Outcome	The student will be able to • Analyze the multimedia networking applications. • Understand the concept of advanced networking. • Understand the concept of traffic modeling. • Learn the scheduling and policing mechanism

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Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE08	**Embedded System Design**	3	0	0	3	50	50	100

Course Objective	• To study the overview of Embedded System Architecture • To provide an in-depth knowledge of embedded system Design. • To study the interfacing Concepts. • To study the design of Software

Unit - I	**EMBEDDED DESIGN LIFE CYCLE**	**Periods**	**09**

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other
issues in selection processes.

Unit - II	**PARTITIONING DECISION**	**Periods**	**09**

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory mapped access – speed and code density.

Unit – III	**INTERRUPT SERVICE ROUTINES**	**Periods**	**09**

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyzer – Caches – Computer optimization – Statistical profiling

Unit – IV	**IN CIRCUIT EMULATORS**	**Periods**	**09**

Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

Unit - V	**TESTING**	**Periods**	**09**

Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

Total Periods	**45**

REFERENCES:

1	Arnold S. Berger – “Embedded System Design”, CMP books, USA 2002.
2	J.W. Valvano, "Embedded Microcomputer System: Real Time Interfacing", Brooks/Cole, 2000
3	ARKIN, R.C., Behaviour-based Robotics, The MIT Press, 1998
4	Sriram Iyer, “Embedded Real time System Programming”

Course Outcome	• Able to understand the embedded Design life cycle. • Able to analyze partition decision and interrupt service routine • Able to analyze in -circuit emulators area • Able to analyze different types of test.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE09	**RF Microelectronics Chip Design**	3	0	0	3	50	50	100

Course Objective	• To study Resonator-less VCO. • To study Linearization techniques. • To understand the operation of MOS devices. • To learn the basics of Multiple Access techniques

Unit – I	**BASIC CONCEPTS IN RF DESIGN**	Periods	**9**

Complexity - design and applications, Choice of Technology, Basic concepts in RF Design - Non linearly and Time Variance - inter-symbol Interference - random processes and Noise, Definitions of sensitivity and dynamic range - conversion Gains and Distortion.

Unit – II	**COMMUNICATION CONCEPTS**	Periods	**9**

Analog and Digital Modulation for RF circuits - Comparison of various techniques for power efficiency, Mobile RF Communication systems and basics of Multiple Access techniques.

Unit - III	**RECEIVER AND TRANSCEIVER ARCHITECTURES**	Periods	**9**

Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters, BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models, Noise performance and limitation of devices.

Unit - IV	**LOW NOISE AMPLIFIERS AND MIXERS**	Periods	**9**

Basic blocks in RF systems and their VLSI implementation- Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range, Various Mixers, their working and implementations.

Unit - V	**OSCILLATORS**	Periods	**9**

Cross Coupled oscillator, three point oscillator, voltage controlled oscillator – LC VCOs with wide tuning range, Phase noise, Design procedures.

	Total Periods	**45**

REFERENCES:

1.	T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004 .
2.	B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3.	Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4.	B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

Course Outcome	The students will be able to • Design various types of oscillators used in chip design • Explain various features of low noise amplifiers. • Sketch the Layout of simple transceiver architectures • Micro electronics chip designing knowledge skills get improved

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE10	**CMOS Analog VLSI Design**	3	0	0	3	50	50	100

Course Objective	• To study the basic CMOS analog circuits. • To understand the concept of Current Source, sink and Reference Circuits. • To design CMOS Amplifiers and converters. • To study IC packaging and process technology

Unit – I	**DYNAMIC ANALOG CIRCUITS**	Periods	**9**

MOSFET Small Signal Model-MOSFET as a Switch- Switched Capacitor Integrator-MOS Diode/Resistor-Resistor Realization using Switched Capacitor-Switched Capacitor Filter- Comparator-D/A and A/D Converter, PLL, Field Programmable Analog Array.

Unit – II	**CURRENT SOURCE-SINK AND REFERNCES**	Periods	**9**

The Current Mirror: The Cascode Connection-Sensitivity Analysis-Temperature Analysis-Transient Response-Layout of the Simple Current Mirror-matching in MOSFET Mirrors-References: Voltage Dividers-Current Source Self Biasing: Threshold Voltage Referenced Self-Biasing-Diode Referenced Self-Biasing-Thermal Voltage Refrenced Self Biasing-Bandgap Voltage References-Beta Multiplier Referenced Self Biasing.

Unit – III	**CMOS ANALOG AMPLIFIERS**	Periods	**9**

Amplifiers: Gate-Drain Connected Loads-Current Source Loads-Noise and Distortion in Amplifiers-Feedback Amplifiers: Properties of Negative Feedback on Amplifier Design-Recognizing Feedback Topologies-Voltage Amplifier- Transimpedance Amplifier –Transconductance Amplifier – Current Amplifier-Output Amplifier -Cascode Amplifiers- Source Follower-Voltage Level Shifter-CMOS Operational Amplifier-Differential Amplifier.

Unit – IV	**DATA CONVERTERS AND ARCHITECTURES**	Periods	**9**

Analog Versus Discrete Time Signals- S/H Characteristics- Mixed Signal Layout Issues-DAC Specifications and Architectures: Digital Input Code- Resistor String-R-2R Ladder networks-Current Steering-Charge Scaling DACs-Cyclic DAC- Pipeline DAC- ADC Specifications and Architectures: Flash-Two-Step Flash ADC-Pipeline ADC-Integrating ADC-Successive Approximation ADC-Oversampling ADC.

Unit - V	**IC PACKAGING AND PROCESS TECHNOLOGY**	Periods	**9**

IC Packaging: Types and Modelling-Electrical Package Modelling- Thermal Modelling- Stress Modelling-Package Simulation- Flip-Chip Package- VLSI Process Technology: Chrystal Growth- Photolithography-Oxidation- Diffusion- Ion Implantation- Etching- Epitaxial Growth- Metallization- Packaging.

Total Periods	**45**

REFERENCES:

1.	R.Jacob Baker, Harry W.Li, David E.Boyce,"CMOS Circuit Design, Layout and Simulation",IEEE Press Series on Microelectronics Systems Stuart K. Tewksbuy, Series Edition.
2.	Debaprasad Das,"VLSI Design" Oxford University Press
3.	Neil H.E.Weste,David Harris, Ayan Banerjee,"CMOS VLSi Design", Pearson, Third Edition.
4.	Malcom R.Haskard, LanC.May,"AnalogVLSIDesign- NMOSandCMOS",PrenticeHall,1998.

Course outcome	The student will be able to • Ability to know about importance of CMOS analog amplifiers and its types. • The ability to understand the need for data converters. • The ability to know the concepts used in CMOS analog VLSI design. • The ability to learn the DAC &ADC architecture.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**
Department	**APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**-**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE11	**Reliability Engineering**	3	0	0	3	50	50	100

Course Objective	• Apply engineering knowledge to prevent or reduce frequency of failures. • To Identify and correct the causes of the failures. • To define methods to mitigate the failures that occur if their causes have not been corrected. • Apply techniques to estimate the reliability of new designs and analyze reliability data.

Unit - I	**PROBABILITY PLOTTING AND LOAD-STRENGTH**	Periods	**9**

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

Unit - II	**RELIABILITY PREDICTION, MODELLING AND DESIGN**	Periods	**9**

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

Unit - III	**ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY**	Periods	**9**

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

Unit - IV	**RELIABILITY TESTING AND ANALYSIS**	Periods	**9**

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

Unit - V	**MANUFACTURE AND RELIABILITY MAQNAGEMENT**	Periods	**9**

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

	Total Periods	**45**

REFERENCES:

1.	Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2.	David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3.	Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", JohnWiley & Sons, New York, 2000

Course Outcome	• Able to apply engineering knowledge to prevent or reduce frequency of failures. • Able to Identify and correct the causes of the failures. • Define methods to mitigate the failures that occur if their causes have not been corrected. • Able to apply techniques to estimate the reliability of new designs and analyze reliability data.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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		L	T	P	C	CA	ESE	Total
P15AEE12	**VLSI Signal Processing**	3	0	0	3	50	50	100

Course Objective	• To study the DSP Systems, Pipelining and parallel processing of FIR Filters. • To understand the concept of Retiming, Algorithmic strength reduction. • To explore the Fast Convolution, Pipelining and Parallel Processing of IIR Filters. • To understand Scaling, Round-Off Noise, Bit-Level Arithmetic Architectures and Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining.

Unit - I	**INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**	Periods	**9**

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

Unit - II	**RETIMING, ALGORITHMIC STRENGTH REDUCTION**	Periods	**9**

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

Unit - III	**FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**	Periods	**9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

Unit - IV	**SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES**	Periods	**9**

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

Unit - V	**NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING**	Periods	**9**

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

Total Periods	**45**

REFERENCES:

1.	Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ",Wiley, Inter science, 2007.
2.	U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.
Course Outcome	The student will be able to • Learn DSP algorithms. • Understand and analysis the concept of pipelining and other processing for DSP applications. • Construct FIR digital filters • Develop Longest path Matrix algorithm

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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Course code	Course name	Periods per week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE13	**ASIC Design**	3	0	0	3	50	50	100
Course Objective	• To study about ASIC fundamentals. • To study different level of ASIC flow . • To explore modeling of ASIC design. • To study FPGA partitioning.							
Unit – I	**INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN**				Periods	**9**		
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.								
Unit – II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**				Periods	**9**		
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.								
Unit – III	**PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY**				Periods	**9**		
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.								
Unit – IV	**LOGIC SYNTHESIS, SIMULATION AND TESTING**				Periods	**9**		
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.								
Unit – V	**ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING**				Periods	**9**		
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.								
					Total Periods	**45**		

REFERENCES:

1.	M.J.S .Smith, “Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.
2.	Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3.	S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4.	Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5.	S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.

6.	Jose E. France, Yannis Tsividis,"Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
Course Outcome	•Able to understand ASICS, CMOS logic and ASIC library design •Able to analyze altera MAX 9000 •Able to analyze the VHDL and logic synthesis •Able to understand the ASIC construction

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE14	**Foundations of VLSI CAD**	3	0	0	3	50	50	100
Course Objective	• To provide an in-depth knowledge in VLSI Design methodology. • To study design rules • To Analysis different types of floor planning, placement and routing algorithms. • To learn the two level logic synthesis and binary decision diagrams.							
Unit – I	**VLSI DESIGN METHODOLOGIES**				Periods	**9**		
Introduction to VLSI Design methodologies - Review of Data structures and algorithms -Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.								
Unit – II	**DESIGN RULES**				Periods	**9**		
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.								
Unit – III	**FLOOR PLANNING**				Periods	**9**		
Floor planning concepts - shape functions and Floor plan sizing - Types of local Routing problems - Area routing - channel routing - global routing - algorithms for global routing.								
Unit – IV	**SIMULATION**				Periods	**9**		
Simulation - Gate-level modelling and simulation - Switch-level modelling and simulation- Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.								
Unit – V	**MODELLING AND SYNTHESIS**				Periods	**9**		
High level Synthesis - Hardware models - Internal representation - Allocation -assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.								
					Total Periods	**45**		
REFERENCE:								
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002							
FURTHER READING:								
1.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.							
Course Outcome	Students will be able to • Analyze the design rules and layout diagram • Analyze the physical design process of VLSI design flow. • Synthesis VLSI Architecture and design integrated circuits • View VLSI design from a hierarchical viewpoint							

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE15	**Power Electronics**	3	0	0	3	50	50	100
Course Objective	• To get an overview of different types of power semi-conductor devices and their switching characteristics. • To understand the operation, characteristics and performance parameters of controlled rectifiers. • To study the operation, switching techniques and basic topologies of DC-DC switching regulators. • To learn the different modulation techniques of pulse width modulated inverters and to understand the harmonic reduction methods. • To study the operation of AC voltage controller and Matrix converters.							
Unit – I	**POWER SEMI-CONDUCTOR DEVICES**					Periods		**9**
Study of switching devices, - Frame, Driver and snubber circuit of SCR, TRIAC,BJT, IGBT, MOSFET,- Turn-on and turn-off characteristics, switching losses, Commutation circuits for SCR.								
Unit – II	**PHASE-CONTROLLED CONVERTERS**					Periods		**9**
Bipolar transistor action, minority carrier distribution, low frequency common-base current gain, non ideal effects, equivalent circuit models, frequency limitations, large signal switching.								
Unit – III	**DC TO DC CONVERTER**					Periods		**9**
Step-down and step-up chopper - Time ratio control and current limit control – Buck, boost, buck- boost converter, concept of Resonant switching - SMPS.								
Unit – IV	**INVERTERS**					Periods		**9**
Single phase and three phase (both 120^0 mode and 180^0 mode) inverters - PWM techniques: Sinusoidal PWM modified sinusoidal PWM - multiple PWM – Introduction to space vector modulations - Voltage and harmonic control - Series resonant inverter - Current source inverter.								
Unit – V	**AC to AC CONVERTERS**					Periods		**9**
Single phase AC voltage controllers – Multistage sequence control - single and three phase cyclo converters –Introduction to Integral cycle control, Power factor control and Matrix converters.								
						Total Periods		**45**
REFERENCES:								
1.	M.H. Rashid, 'Power Electronics: Circuits, Devices and Applications', Pearson Education, PHI Third edition, New Delhi 2004.							
2.	Philip T.Krein, "Elements of Power Electronics" Oxford University Press, 2004 Edition.							
FURTHER READINGS:								
1.	Ashfaq Ahmed Power Electronics for Technology Pearson Education, Indian reprint, 2003.							
2.	P.S.Bimbra "Power Electronics" Khanna Publishers, third Edition 2003.							
3.	Ned Mohan, Tore.M.Undeland, William.P.Robbins, 'Power Electronics: Converters, Applicatio and Design', John Wiley and sons, third edition, 2003.							

Course Outcome	• Gives an overview of different types of power semi-conductor devices and their switching characteristics. • Understand the operation, characteristics and performance parameters of controlled rectifiers. • Analyze the operation, switching techniques and basic topologies of DC-DC switching regulators. • Able to learn the different modulation techniques of pulse width modulated inverters and to understand the harmonic reduction methods. • Able to study the operation of AC voltage controller and Matrix converters.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**COMPUTER SCIENCE, VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**-**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE16	**Computer Architecture and Parallel Processing**	3	0	0	3	50	50	100
Course Objective	• To understand Computer Design and Architecture. • To understand the state-of-the-art in parallel processing and computer hardware technologies. • To study theory of parallelism. • To study pipelining and superscalar technologies in parallel processing							
Unit – I	**THEORY OF PARALLELISM**				Periods	**9**		
Parallel computer models - the state of computing, Multiprocessors and Multicomputer and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.								
Unit – II	**PARTITIONING AND SCHEDULING**				Periods	**9**		
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.								
Unit – III	**HARDWARE TECHNOLOGIES**				Periods	**9**		
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.								
Unit – IV	**PIPELINING AND SUPERSCALAR TECHNOLOGIES**				Periods	**9**		
Parallel and scalable architectures, Multiprocessor and Multicomputer, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.								
Unit – V	**SOFTWARE AND PARALLEL PROGRAMMING**				Periods	**9**		
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.								
					Total Periods	**45**		

REFERENCES:

1.	Kai Hwang, "Advanced Computer Architecture ", McGraw Hill International, 2001.

FURTHER READINGS:

1.	Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach" , Pearson Education , 2003.
2.	John P.Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003.
3.	John P.Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003.
4.	Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Tata Mc-Graw Hill, 5th Edition,2002.

Course Outcome	• able to Analyze the different types of Architectures • able to learn about pipelining and superscalar technologies • able to understand and analysis about the software and parallel programming for various industry based applications • Identification of new developments in Computer Architecture and Parallel Processing

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE17	**Pattern Recognition & Artificial Intelligence**	3	0	0	3	50	50	100
Course Objective	• To understand different supervised and unsupervised learning techniques • To obtain sound knowledge on recent advancement on pattern recognition techniques. • To study hierarchical clustering procedures • To study Neural network based Pattern associators.							
Unit – I	**PATTERN CLASSIFIER**				Periods	**9**		
Overview of pattern recognition - Discriminant functions - Supervised learning - Parametric estimation - Maximum likelihood estimation - Bayesian parameter estimation - Perceptron algorithm - LMSE algorithm- Problems with Bayes approach - Pattern classification by distance functions - Minimum distance pattern classifier								
Unit – II	**UNSUPERVISED CLASSIFICATION**				Periods	**9**		
Clustering for unsupervised learning and classification - Clustering concept - C-means algorithm – Hierarchical clustering procedures - Graph theoretic approach to pattern clustering - Validity of clustering solutions.								
Unit – III	**STRUCTURAL PATTERN RECOGNITION**				Periods	**9**		
Elements of formal grammars - String generation as pattern description - Recognition of syntactic description -Parsing - Stochastic grammars and applications - Graph based structural representation.								
Unit – IV	**FEATURE EXTRACTION AND SELECTION**				Periods	**9**		
Entropy minimization - Karhunen - Loeve transformation - Feature selection through functions approximation -Binary feature selection.								
Unit – V	**RECENT ADVANCES**				Periods	**9**		
Neural network structures for Pattern Recognition - Neural network based Pattern associators – Unsupervised learning in neural Pattern Recognition - Self organizing networks - Fuzzy logic - Fuzzy pattern classifiers -Pattern classification using Genetic Algorithms.								
					Total Periods	**45**		
REFERENCES:								
1	Robert J.Schalkoff, Pattern Recognition: Statistical, Structural and Neural Approaches, John Wiley &Sons Inc., New York, 2007.							
2	Tou and Gonzales, Pattern Recognition Principles, Wesley Publication Company, London, 1974							
3	Duda R.O., Hart.P.E., and Strok, Pattern Classification, second Edition Wiley, New York, 2008							
4	Morton Nadier and Eric Smith P., Pattern Recognition Engineering, John Wiley & Sons,							

	New York, 1993
FURTHER READINGS:	
1.	IEEE Transaction on Pattern Recognition Techniques 2006
2.	IEEE Engineering Medicine and Biology Magazine 2006.
Course Outcome	The student will be able to • Analyze the procedure for various pattern recognition principles in real world problem. • Identification of new developments in object recognition systems. • Learn the structural pattern recognition methods • Understand the concept of Pattern classification using Genetic Algorithms

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Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**-**			
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE18	**Soft Computing**	3	0	0	3	50	50	100

Course Objective	• .To learn the key aspects of Soft computing and Neural networks. • To know about the components and building block hypothesis of Genetic algorithm. • To understand the features of neural network and its applications • To study the fuzzy logic components • To gain insight onto Neuro Fuzzy modeling and control.

Unit – I	**ARTIFICIAL NEURAL NETWORKS**	Periods	**9**

Supervised learning Neural networks-Introduction, Perception- Adaline, Back propagation- Multilayer perception- Unsupervised learning and other Neural networks-Introduction, Competitive learning networks, Kohenen self organizing networks, Learning vector quantization, Hebbian learning, Hopfield network , Content addressable nature, Binary Hopfield network, Continuous- valued Hopfield network , Travelling Salesperson problem.

Unit – II	**FUZZY SET THEORY**	Periods	**9**

Fuzzy sets, Basic definitions and terminology, Member function formulation & parameterization, Fuzzy rules , fuzzy reasoning - Extension principle, Fuzzy relation, Fuzzy inference systems:Mamdani model, Sugeno model. Tsukamoto model, Input space partitioning, Fuzzy modeling.

Unit – III	**OPTIMIZATION**	Periods	**9**

Derivative based optimization-Descent methods, Method of steepest descent, Classical Newtons method, Step-size determination; Derivative free optimization- Genetic algorithm, Simulated annealing, Random search, Downhill search.

Unit – IV	**ADVANCED NEURO-FUZZY MODELLING**	Periods	**9**

Classification and regression trees, decision tress, Cart algorithm – Data clustering algorithms: K-means clustering, Fuzzy C-means clustering, Mountain clustering, Subtractive clustering – rulebase structure, Input space partitioning, rule based organization, focus set based rule combination; Neuro-fuzzy control: Feedback Control Systems, Expert Control, Inverse Learning, SpecializedLearning, Back propagation through real time Recurrent Learning.

Unit – V	**GENETIC ALGORITHM**	Periods	**9**

Fundamentals of genetic algorithm- Basic concepts - Encoding – Binary, Octal, Hex, Permutation,Value and tree, Reproduction- Roulette-wheel selection, Boltzman selection, Tournament selection, Rank selection, Steady state selection, Crossover single site, Two point, Multi point, Uniform and matrix, Crossover rate, Inversion, Deletion and duplication, Deletion and Regeneration, Segregation, Crossover, Mutation, Generational cycle.

Total Periods	**45**

REFERENCES:

1. Jang J.S.R.,Sun C.T and Mizutani E, "Neuro Fuzzy and Soft computing", Pearson education (Singapore) 2004.

FURTHER READINGS:

1. S.Rajasekaran and G.A.Vijayalakshmi Pai, "Neural networks,Fuzzy logics,and Genetic Algorithms", Prentice Hall of India, 2003.

2.	David E.Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning",Pearson Education, Asia,1996
3.	Laurene Fauseett, ''Fundamentals of Neural Networks", Prentice Hall India, NewDelhi,1994
4.	Timothy J.Ross, ''Fuzzy Logic Engineering Applications", McGrawHill,NewYork,1997
Course Outcome	• Implement machine learning through Neural networks. • Develop a Fuzzy expert system. • Model Neuro Fuzzy system for clustering and classification. • Write Genetic Algorithm to solve the optimization problem • Use Support Vector Machine for enabling the machine learning

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	-		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE19	**Neural Networks and its Applications**	3	0	0	3	50	50	100
Course Objective	• To study the basic network learning algorithms. • To understand the concept of radial basis networks and functions. • To study committee machines and neuro dynamics systems. • To study attractor neural networks and adaptive resonance theory. • To understand the concept of self organizing maps and pulsed neuron models.							
Unit - I	**BASIC LEARNING ALGORITHMS**				Periods	**9**		
Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feed forward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering-Beam forming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.								
Unit - II	**RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES RADIAL BASIS FUNCTION NETWORKS**				Periods	**9**		
Cover's Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification. Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - □-insensitive Loss Function – Support Vector Machines for Nonlinear Regression.								
Unit - III	**COMMITTEE MACHINES**				Periods	**9**		
Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model. **NEURODYNAMICS SYSTEMS:** Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems- Lyapunov Stability – Neuro dynamical Systems – The Cohen-Gross berg Theorem.								
Unit - IV	**ATTRACTOR NEURAL NETWORKS**				Periods	**9**		
Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks- Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine –								

Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications **ADAPTIVE RESONANCE THEORY:** Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center – Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications			
Unit - V	**SELF ORGANISING MAPS**	Periods	**9**
Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications **PULSED NEURON MODELS:** Spiking Neuron Model – Integrate-and-Fire Neurons – Conductance Based Models – Computing with Spiking Neurons			
		Total Periods	**45**
REFERENCES:			
1.	Satish Kumar, "Neural Networks: A Class room Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.		
2.	Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.		
3.	Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.		
4.	James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) PrivateLimited, Delhi, 2003.		
Course Outcome	The student will be • Able to identify the various challenges in Neural Networks. • Able to analyze the performance attractor neural networks. • Able to understand the characteristics of committee machines • Able to estimate the performance and throughput of a given network.		

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-			

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE20	**Nano Electronics**	3	0	0	3	50	50	100

Course Objective	• To acquire knowledge about fundamental quantum mechanics. • To study about architecture and operations of different nano structures. • To comprehend the low dimension, high speed and low power design techniques and methodologies. • To study photonic networks.

Unit - I	**TECHNOLOGY AND ANALYSIS**	Periods	**9**
Film Deposition Methods – Lithography- Material removing techniques - Etching and Chemical-Mechanical Polishing - Scanning Probe Techniques.			
Unit - II	**CARBON NANO STRUCTURES**	Periods	**9**
Carbon Clusters - Carbon Nano tubes – Fabrication – Electrical, Mechanical and Vibrational Properties – Applications of Carbon Nano tubes.			
Unit - III	**LOGIC DEVICES**	Periods	**9**
Silicon MOSFET's – Novel materials and alternative concepts – Ferroelectric Field Effect Transistors – Super conductor digital electronics – Carbon Nano tubes for data processing.			
Unit - IV	**RANDOM ACCESS MEMORIES AND MASS STORAGE DEVICES**	Periods	**9**
High Permittivity material for DRAM's – Ferro electric Random Access memories – Magneto- resistive RAM- Hard Disk Drives – Magneto Optical Disks – Rewriteable DVDs based on Phase Change Materials – Holographic Data Storage.			
Unit - V	**DATA TRANSMISSION AND INTERFACES AND DISPLAYS**	Periods	**9**
Photonic Networks – Microwave Communication System – Liquid Crystal Displays – Organic Light emitting diodes.			
		Total periods	**45**

REFERENCES:

1.	Rainer Waser, Nano Electronics and Technology, Wiley VCH, 2003.
2.	Charles Poole, Introduction to Nano Technology, Wiley Inter science, 2003.
3.	C.Wasshuber, Simon , Simulation of Nano Structures Computational Single-Electronics, Springer-Velag,2001.
4.	Rainer Waser, Nano Electronics and information technology advanced electronic materials and novel devices, Wiley –VcH Verlag GmBh-KgaH, Germany, 2005.
5.	A. Mark Reed and Takhee Lee, Molecular Nano Electronics, American Scientific Publisher, California, 2003.

Course Outcome	• Comprehend fundamental quantum mechanics. • Able to study about architecture and operations of different Nano structures. • Comprehend the low dimension, high speed and low power design techniques and methodologies. • Able to Understand data transmission techniques.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS&VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	-		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE21	**System Design Using FPGA**	3	0	0	3	50	50	100

Course Objective	• To study PLA and PLE. • To understand the concept of configurable logic blocks. • To study Xilinx CAD tools. • To study the general concepts in testing

Unit – I	**PROGRAMMABLE LOGIC DEVICES& FPGA**	Periods	**9**
Introduction to FPGA- FPGA vs Custom VLSI- FPGA Design Flow- Basic concepts - Programming techniques -Programmable Logic Element (PLE) -Programmable Logic Array (PLA) - Programmable Array Logic (PAL) –CPLDs- CPLD Architectures- CPLD Design Flow- Comparison with FPGAs.			
Unit – II	**FIELD PROGRAMMABLE GATE ARRAYS (FPGAS)**	Periods	**9**
FPGA Architectures- Configurable Logic Blocks (CLB) - Xilinx XC3000, Xilinx XC4000, Xilinx XC5200 series- Configurable I/O Blocks (I/OB)- Programmable Interconnect- Technology Issues.			
Unit – III	**FPGA DESIGN FLOW**	Periods	**9**
Design Entry- Functional Simulation- Technology Mapping- Synthesis- Timing Simulation- Verification- Implementation.			
Unit – IV	**DESIGN TECHNIQUES, RULES, AND GUIDELINES**	Periods	**9**
Verilog -Hardware Description Languages-Various Levels of Modeling-Top-Down Design-Synchronous Design- Xilinx CAD Tools-with design examples.			
Unit – V	**VERIFICATION AND TESTING**	Periods	**9**
Introduction about General concepts in testing -Design For Test (DFT)- Built-In Self-Test (BIST))- SignatureAnalysis- Static Timing Analysis- Formal Verification.			
		Total Periods	**45**

REFERENCES:

1	Bob Zeidman, Designing with FPGAs and CPLDs, Elsevier, CMP Books, 2002
2	Ion Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier, 2008
3	Samir Palnitkar, Verilog HDL, Pearson Education, 2nd Edition, 2004
4	Michael john Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley, Ninth IndianReprint, 2004

FURTHER READINGS:

1.	W.Wolf, FPGA- based System Design, Pearson, 2004.
2.	Michael L. Bushnell and Vishwani D. Agarwal, Essentials of Electronic Testing for Digital and MixedSignal VLSI Circuits, Springer, 2000.

Course Outcome	• Ability to identify the various challenges in FPGA • Able to Understand and recognize the design techniques ,rules and guidelines • Able to Analyze the FPGA design flow • Able to understand technology issues

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-			

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE22	**DSP Processor Architecture and Programming**	3	0	0	3	50	50	100

Course Objective	• To Study the fundamentals of Programmable DSPs. • To Impart knowledge on the operation of ADSP and Analog Processors • To study TMS320C5X processor • To study ADSP Processors

Unit – I	**FUNDAMENTALS OF PROGRAMMABLE DSPS**	Periods	**9**
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSPs – Multiple access memory– Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in PDSPs– On chip Peripherals.			
Unit – II	**TMS320C5X PROCESSOR**	Periods	**9**
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure– Operation – Programs for FIR and IIR filters.			
Unit – III	**TMS320C3X PROCESSOR**	Periods	**9**
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation–Generating and finding the sum of series- Convolution of two sequences- Programs for FIR and IIR filters.			
Unit – IV	**ADSP PROCESSORS**	Periods	**9**
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assemblylanguage instructions – Application programs – Programs on ADSP21xx for FIR and IIR filters			
Unit – V	**ADVANCED PROCESSORS**	Periods	**9**
Architecture of TMS320C54X - Pipe line operation, Code Composer studio - Architecture of TMS320C6X -Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.			
		Total Periods	**45**

REFERENCES:

1	B.Venkataramani. and M.Bhaskar, Digital Signal Processors – Architecture, Programming andApplications, Tata McGraw – Hill Publishing Company Limited, 2003.
2	User guides of Texas Instruments, Analog Devices, Motorola Incorporation, 2005

Course Outcome	• Analyse the procedure for various DSP System Architecture • Diagnose the design methodologies in hardware and software. • Identification of new developments in DSP systems. • Design and implement various signal processing techniques using DSP processors

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation	**2015**		
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester	-		
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE23	**Embedded Systems in Automotive Applications**	3	0	0	3	50	50	100

Course Objective	• To Study the fundamentals of embedded systems • To Impart knowledge on the operation of various sensors • To study the operating system in embedded environment • To study the communication protocols and applications

Unit – I	**AUTOMOBILE ELECTRICAL AND ELECTRONICS**	Periods	**9**
Basic Electrical Components and their operation in an automobile - Starting systems, Charging systems – ignition systems- Electronic fuel control- Environmental legislation for pollution- Overview of vehicle electronic systems- Power train subsystem- chassis subsystem- comfort and safety subsystems.			
Unit – II	**INTRODUCTION TO EMBEDDED SYSTEMS**	Periods	**9**
Embedded Systems definition - Components of Embedded systems – Microprocessor - Classification of Microprocessors- Microcontrollers- Memory - Peripherals. Introduction to an embedded board (TMS470 based / ARM9 based) for hands on lab sessions (RISC processor based with standard peripherals / interfaces and I/Os)			
Unit – III	**OPERATING SYSTEM IN EMBEDDED ENVIRONMENT**	Periods	**9**
Introduction to OS - General Purpose OS, RTOS -, Kernel - Pre-emptive & Non pre-emptive,Scheduler, Interrupt - Interrupt latency and Context Switch Latency- Board Support package, Task- Multi-tasking, Task synchronization, Inter-task communication, Features of a typical embeddedRTOS (µC/OS-II)			
Unit – IV	**INTEGRATED DEVELOPMENT ENVIRONMENT**	Periods	**9**
Integrated Development Environment (IDE)- Getting Started, Hardware / Software Configuration(Boot Service, Host – Target Interaction), Booting, Reconfiguration, Managing IDE, Target Servers, Agents, Cross – Development, debugging- Introduction to an IDE for the lab board – RTOS, PC based debugger.			
Unit – V	**COMMUNICATION PROTOCOLS AND APPLICATIONS**	Periods	**9**
Engine Management systems - Diesel / Gasoline systems, Various sensors used in system -Vehicle safety systems- electronic control of braking and traction- Introduction to control elements and control methodology- Electronic transmission control- Body electronics - Infotainment systems– Navigation systems- Introduction to CAN, LIN, FLEXRAY, MOST, KWP 2000 Protocols			
		Total Periods	**45**

REFERENCES:

1	R. K. Jurgen, "Automotive electronics handbook" McGraw Hill Professional, 1999
2	Paul Pop, Petru Eles, Zebo Peng ''Analysis and Synthesis of Distributed Real-Time Embedded Systems'' Springer, 21-Dec-2004
3	B. Kanta Rao ''Embedded Systems'' PHI Learning Pvt. Ltd.2011

Course Outcome	• Able to learn the communication protocols used in embedded system • Able to analyze the PC based debugger • Able to understand the concept of RTOS • Able to study the vehicle electronic systems

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**	Regulation	**2015**			
Department	**APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	-			

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE24	**Medical Image Processing**	3	0	0	3	50	50	100

Course Objective	• To study about various medical image acquisition methods. • To understand 2D and 3D image reconstruction techniques. • To gain sound knowledge about CT, MRI, nuclear and ultrasound imaging. • To realize the factors those affect the quality of medical images.

Unit – I	**ACQUISITION OF IMAGES**	Periods	**9**

Introduction to Imaging Techniques- Single crystal scintillation camera – Principles of scintillation camera – multiple crystal scintillation camera –solid state camera –rectilinear scanner –Emission computed Tomography.

Unit – II	**MATHEMATICAL PRELIMINARIES FOR IMAGE RECONSTRUCTION**	Periods	**9**

Image Reconstruction from Projections in Two dimensions –Mathematical Preliminaries for Two and Three dimensional Image Reconstructions –Radon Transform –Projection Theorem –central slice Theorem – Sinogram – Two Dimensional Projection Reconstruction –Three Dimensional Projection Reconstruction – Iterative Reconstruction Techniques.

Unit – III	**FLUOROSCOPY, CT, IMAGE QUALITY**	Periods	**9**

Digital fluoroscopy – Automatic Brightness control- cinefluorography –Principles of computed Tomographic Imaging- Reconstruction algorithms- Scan motions – X –ray sources **Influences of Images quality:**Unsharpness – contrast- Image Noise.

Unit – IV	**MAGNETIC RESONANCE IMAGING AND SPECTROSCOPY**	Periods	**9**

Fundamentals of magnetic resonance – overview – Pulse techniques – spatial encoding of magnetic resonance imaging signal – motion suppression techniques – contrast agents- tissue contrast in MRI – MR angiography, spectrography.

Unit – V	**ULTRA SOUND, NEURO MAGNETIC IMAGING**	Periods	**9**

ultra Sound: Presentation modes – Time required to obtain Images – System components, signal processing –dynamic Range – Ultrasound Image Artifacts – Quality control, Origin of Doppler shift – Limitations of Doppler systems. **Neuromagnetic Imaging:** Background

Total Periods	**45**

REFERENCES:

1	William R. Hendee, E. Russell Ritenour, Medical Imaging Physics: A John Wiley & sons, Inc.,Publication, Fourth Edition 2002.
2	Z.H. Cho., J-oie, P. Jones and Manbir Singh, Foundations of Medical Imaging: John Wiley and sons Inc.
3	Avinash C. Kak, Malcolm Shaney, Principles of Computerized Tomographic Imaging, IEEEPress, Newyork-1998.

Course Outcome	• Bring out the procedure for medical image acquisitions. • Describe and determine the performance of different Image reconstruction techniques. • Analysis the physiological events associated with the human system. • Describe the influences of artifacts in image quality • Identification of new developments in health care system

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205							
Programme	**M.E.**	Programme Code	**203**		Regulation		**2015**	
Department	**APPLIED ELECTRONICS/ ELECTRONICS AND COMMUNICATION ENGINEERING**				Semester		**-**	
Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P15AEE25	**Robotics**	3	0	0	3	50	50	100
Course Objective	• To study the fundamental concepts of kinematics. • To gain the knowledge about various sensors used in robotics. • By combining the concepts of computer vision and AI techniques to design a robot. • To study sensors and sensing devices							
Unit – I	**INTRODUCTION TO ROBOTICS**					Periods		**9**
Robotic Classification, Robot Specifications, Motion – Bug and tangent algorithms, Potential Function, Road maps- Topological roadmaps, Cell decomposition – Trapezoidal and Morse cell decompositions , Sensor and sensor planning- Kinematics-Forward and Inverse Kinematics - Transformation matrix and DH transformation-Inverse Kinematics - Geometric methods and Algebraic methods.								
Unit – II	**COMPUTER VISION**					Periods		**9**
Projection - Optics, Projection on the Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling, Thresholding, Histogram-Convolution - Digital Convolution and Filtering and Masking Techniques- Edge Detection - Mono and Stereo Vision.								
Unit – III	**SENSORS AND SENSING DEVICES**					Periods		**9**
Introduction to various types of sensor- Resistive sensors. Range sensors - LADAR (Laser Distance and Ranging), Sonar, Radar and Infra-red- Introduction to sensing - Light sensing, Heat sensing, touch sensing and Position sensing.								
Unit - IV	**ARTIFICIAL INTELLIGENCE**					Periods		**9**
Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth first search and Bidirectional search. The A* algorithm-Planning - State-Space Planning Plan-Space Planning, Graph plan/Sat Plan and their Comparison, Multi-agent planning 1, and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference.								
Unit - V	**INTEGRATION TO ROBOT**					Periods		**9**
Building of 4 axis or 6 axis robot - Vision System for pattern detection - sensors for obstacle detection – AI algorithms for path finding and decision making.								
						Total Periods		**45**
REFERENCES:								
1.	Duda, Hart and Stork, Pattern Recognition, Wiley-Inter science, 2000.							
2.	Mallot, Computational Vision: Information Processing in Perception and Visual Behavior, Cambridge, 2000.							

3.	Stuart Russell and Peter Norvig, Artificial Intelligence-A Modern Approach, Pearson Education Series in Artificial Intelligence, 2004.
4.	Robert Schilling and Craig, Fundamentals of Robotics: Analysis and Control, Hall of India Private Limited, 2003.
5.	Forsyth and Ponce, Computer Vision: A Modern Approach, Person Education, 2003.
Course Outcome	• Able to study the fundamental concepts of kinematics. • Able to gain the knowledge about various sensors used in robotics. • Designing the Robot by combining the concepts of computer vision and AI techniques • Able to understand the concept of artificial intelligence

Annexure-I

List of Service Courses

Programme: **M.E - APPLIED ELECTRONICS**

Semester	Course Code	Course Name	Service Programme
-	-	-	-

Annexure-II

List of Common Courses

Programme: **M.E – APPLIED ELECTRONICS**

Semester	Course Code	Course Name	Common to			
			Programme	Semester	Course Code	Course Name
I	P15AE101	Advanced Digital System Design	M.E .VLSI DESIGN	I	P15VD101	Advanced Digital System Design
I	P15AE103	Advanced Digital Signal Processing	M.E .VLSI DESIGN	-	P15VDE03	Advanced Digital Signal Processing
-	P15AEE02	VLSI Design	M.E .VLSI DESIGN	-	P15VDE06	VLSI Design
-	P15AEE06	Low Power VLSI Design	M.E .VLSI DESIGN	II	P15VD206	Low Power VLSI Design
-	P15AEE10	CMOS Analog VLSI Design	M.E .VLSI DESIGN	I	P15VD104	CMOS Analog VLSI Design
-	P15AEE08	Embedded System Design	M.E .VLSI DESIGN	-	P15VDE09	Embedded System Design
-	P15AEE09	RF Microelectronics Chip Design	M.E .VLSI DESIGN	-	P15VDE04	RF Microelectronics Chip Design
-	P15AEE12	VLSI Signal Processing	M.E .VLSI DESIGN	-	P15VDE10	VLSI Signal Processing
-	P15AEE14	Foundations of VLSI CAD	M.E .VLSI DESIGN	-	P15VDE07	Foundations of VLSI CAD
-	P15AEE20	Nano Electronics	M.E .VLSI DESIGN	-	P15VDE21	Nano Electronics
-	P15AEE13	ASIC Design	M.E .VLSI DESIGN	-	P15VDE26	ASIC Design
-	P15AEE21	System Design using FPGA	M.E .VLSI DESIGN	-	P15VDE19	System Design Using FPGA
II	P15AE208	Research Methodology and Data analysis	M.E .VLSI DESIGN	II	P15VD208	Research Methodology and Data analysis
			M.E .CSE	II	P15CS209	Research Methodology and Data analysis
			M.E .PSE	II	P15PS208	Research Methodology and Data analysis
			M.Tech. IT	II	P15IT208	Research Methodology and Data analysis