VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
(AUTONOMOUS)
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

ACADEMIC YEAR : 2017-2018 **YEAR : II**
BRANCH : CSE **SEM : 03**
SUBJECT NAME & CODE : DIGITAL LOGIC DESIGN & U15EC305
SUBJECT INCHARGE : Ms. V. ARUL, AP/CSE,

LESSON PLAN

UNIT I

Session No	Topics to be covered	Time In mints	Text/Ref	Teaching Method
1	Introduction of Digital Systems	45	A	BB
2	Number Systems	45	A	BB
3	Number System base conversion	45	A	BB
4	Binary to Decimal conversion	45	A	BB
5	Decimal to octal & Hexa decimal conversion	45	A	BB
6	Problems workout	45	A	BB
7	Signed Binary Numbers	45	A	BB
8	Binary Codes	45	A,B	BB
9	Logic Gates	45	A	BB
10	Problems Workout	45	A,B	BB

UNIT II

Session No	Topics to be covered	Time	Text/Ref	Teaching Method
1	Introduction of Boolean Algebra	45	A	BB
2	Axioms and Laws of Boolean Algebra	45	A	BB
3	Boolean function • Canonical Forms • Standard Forms	45	A	BB
4	Introduction of K-Map	45	A	BB
5	Types of K – Map • One variable K – map • Two variable K - map	45	A	BB
6	Problems workout	45	A,B	BB
7	• Three variable K – map • Four Variable K - map	45	A	BB

8	Problems Workout	45	A,B	BB
9	Don't care Condition	45	A	BB
10	NAND and NOR Implementation	45	A	BB
11	Revision	45	-	BB

UNIT III

Session No	Topics to be covered	Time	Text/Ref	Teaching Method
1	Introduction of Combinational Logic	45	A	BB
2	Logic Circuits	45	A	BB
3	Binary Adder and Subtractor	45	A	BB
4	Problems Workout	45	A,B	BB
5	Look Ahead Carry Adder	45	A	BB
6	Problems Workout	45	A,B	BB
7	Comparators	45	A	BB
8	Decoders	45	A	BB
9	Encoders	45	A,B	BB
10	Multiplexers	45	A,B	BB
11	Demultiplexers	45	A	BB
12	Revision	45	-	BB

UNIT IV

Session No	Topics to be covered	Time	Text/Ref	Teaching Method
1	Introduction of Memory and Programmable Logic Device	45	A	BB
2	Programmable Logic Device • ROM • PROM	45	A	BB
3	Continuity of Programmable Logic Device • EPROM • EEPROM	45	A,B	BB
4	Programmable Logic Array (PLA)	45	A,B	BB

5	Problems Workout	45	A,B	BB
6	Programmable Array Logic (PAL)	45	A	BB
7	Problems Workout	45	A,B	BB
8	Problems Workout	45	A,B	BB
9	Revision	45	A	BB

UNIT V

Session No	Topics to be covered	Time	Text/Ref	Teaching Method
1	Introduction of Synchronous Logic	45	A	BB
2	Over view of Sequential circuits	45	A	BB
3	Latch	45	A	BB
4	Flip Flop • SR Flip Flop • Jk Flip Flop	45	A,B	BB
5	• T Flip Flop • D Flip Flop	45	A,B	BB
6	Execution tables of Flip Flop	45	A	BB
7	Problems Workout	45	A	BB
8	Register and Counters	45	A	BB
9	Shift registers	45	A,B	BB
10	Problems workout	45	A	BB
11	Counters and Ripple Counters	45	A	BB
12	Other Counters	45	A	BB
13	Problems workout	45	A	BB
14	Revision	45	-	BB

Text Book and References :

1.	Digital Logic and Computer Design by M. Moris Mano, 4th Edition.
2.	Digital Principles and Applications by Leach, paul Malvino, 5th Edition
3.	Fundamentals of Digital Logic Design by Charles H. Roth, Jr. 5th Edition, Cengage

SUBJECT IN CHARGE **HOD** **PRINCIPAL**