VIVEKANANDHA
COLLEGE OF ENGINEERING FOR WOMEN
(An Autonomous Institution, Affiliated to Anna University, Chennai)
Elayampalayam,Tiruchengode-637 205
Department of Electronics and Communication Engineering

Lession Plan : U15EC518 - Principles of VLSI Design **III ECE**

Session No.	Topics Covered	Duration in Minutes	Teaching Aid	Books Referred
UNIT I	**INTRODUCTION AND CMOS PROCESS TECHNOLOGY**			
1.	Introduction –VLSI Design, A brief History	45m	BB	1
2.	IC Design techniques	45m	BB	
3.	VLSI design flow	45m	BB	
4.	NMOS, PMOS Enhancement transistor	45m	PPT	1
5.	MOS transistor-Ideal I-V characteristics	45m	PPT	1
6.	MOS transistor C-V characteristics	45m	PPT	1
7.	Non-ideal I-V characteristics- velocity saturation	45m	PPT	1
8.	Threshold voltage, Body effect, Junction leakage,	45m	PPT	1
9.	CMOS inverter DC transfer characteristics, Beta	45m	PPT	1
10.	Switch level RC delay models	45m	BB	
11.	CMOS fabrication methods – P well, N- well, twin	45m	PPT	1,4
12.	CMOS fabrication methods - twin tub, SOI	45m	PPT	
13.	Layout design rules-NAND,NOR gat	45m	PPT	1
14.	CMOS Process enhancement-SOI Process,	45m	PPT	1
15.	CMOS logic	45m	BB	
16.	Circuit element: capacitor, CAD and manufacturing	45m	BB	1,3
UNIT II	**CIRCUIT AND DEVICE CHARACTERIZATION**			
17	Delay estimation-RC delay model, Linear delay	45m	BB	1,4
18	Logical effort	45m	PPT	1,4
19	Transistor sizing	45m	BB	1
20	Power dissipation-static and dynamic power	45m	BB	1
21	Interconnect –Estimation of resistance capacitance,	45m	BB	1,4
22	Design margin	45m	PPT	1
23	Reliability	45m	PPT	1
24	Scaling	45m	PPT	1,4
25	SPICE tutorial, Device models	45m	BB	1
26	Device &Circuit characterization	45m	BB	1
UNIT III	**COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN**			
27	Circuit families-static CMOS, ratioed circuit	45m	BB	1,4
28	Cascode voltage swing logic, Dynamic circuits	45m	BB	1,4
29	Pass transistor, Differential circuits	45m	BB	1
30	BiCMOS, Low power logic design – comparison of	45m	BB	1
31	Sequencing static circuits	45m	BB	1
32	Circuit design of latches and flip flops	45m	PPT	1
33	Static sequencing element	45m	PPT	1

34	Sequencing dynamic circuits	45m	PPT	1
35	Synchronizers	45m	BB	1
36	Data path subsystem design	45m	PPT	1
37	Addition/Subtraction, Comparators.	45m	PPT	1
UNIT IV	**CMOS TESTING**			
38	Need for testing	45m	BB	1
39	Text fixtures and test programs	45m	BB	1
40	Logic verification- Silicon	45m	BB	1
41	Manufacturing test	45m	BB	1,3,4
42	Design for testability-adhoc testing	45m	BB	1
43	Scan design	45m	BB	1
44	Built in self test, IDDQ testing	45m	PPT	1
45	Boundary scan	45m	PPT	1
UNIT V	**SPECIFICATION USING VERILOG HDL**			
46	Basic concepts- identifiers- gate primitives,, Design	45m	BB	5
47	Gate delays	45m	PPT	5
48	Operators	45m	PPT	5
49	Timing controls	45m	PPT	5
50	Procedural assignments conditional statements	45m	BB	5
51	Data flow and RTL	45m	BB	5
52	Structural gate level	45m	BB	5
53	Switch level modeling	45m	PPT	5
54	Behavioral and RTL modeling, Test benches	45m	PPT	5
55	Gate level verilog code-Decoder, equality detector,	45m	PPT	5
56	Half adder, full adder, Ripple carry adder, D latch	45m	PPT	5

TEXT BOOKS:

1. Neil H.E.Weste,David Harris, Ayan Banerjee, "CMOS VLSI Design", Pearson, Third Edition.
2. J.Bhaskar, "verilog HDL Synthesis –A practical printer",(star galaxy publishing:Allentown,PA,1998).

REFERENCES:

3. R.Jacob Baker, Harry W.Li, David E.Boyce,"CMOS Circuit Design, Layout and Simulation",IEEE Press Series on Microelectronics Systems Stuart K. Tewksbuy, Series Edition.
4. Douglas A.Pucknell,Kamran Eshraghian, "Basic VLSI Design" Prentice Hall,Third Edition.
5. Samir Palnitkar "Verilog HDL A Guide to Degital Design and Synthesis" second Edition.

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