LESSON PLAN

Sub Code& Name: U15ECE31 & COMPUTER ARCHITECTURE

Unit : I **Branch : ECE** **Semester: V**

Session No.	Topics to be covered	Duration in Mins	Teaching Method	Books Ref
1.	Introduction to computer types -How it all Started	45m	PPT	1,3,5
2.	Functional unit	45m	PPT	1,2,3
3.	Basic operational concepts	45m	PPT	1,2
4.	Bus structures	45m	PPT	1,2,3
5.	Software	45m	PPT	1,2,3
6.	Performance	45m	PPT	1,2,4
7.	Multiprocessors and multi computers	45m	PPT	1,2
8.	Data Representation	45m	PPT	1,2
9.	Fixed Point Representation	45m	PPT	1,2,3
10.	Floating – Point Representation	45m	PPT	1,2,3
11.	Error Detection codes	45m	PPT	1,2,3
12.	Revision	45m	PPT	-

	LESSON PLAN	
	Sub Code & Name: U15ECE31 & COMPUTER ARCHITECTURE **Unit :II** **Branch : ECE** **Semester: V**	

Session No.	Topics to be covered	Duration in Mins	Teaching Method	Books Ref
1.	Fixed Point Arithmetic	45m	PPT	1,3,5
2.	Addition	45m	PPT	1,2,3
3.	Subtraction	45m	PPT	1,2
4.	Multiplication and Division	45m	PPT	1,2,3
5.	Combinational and Sequential ALUs	45m	PPT	1,2,3
6.	Carry look ahead adder,	45m	PPT	1,2,4
7.	Robertson algorithm	45m	PPT	1,2
8.	booth's algorithm	45m	PPT	1,2
9.	non- restoring division algorithm	45m	PPT	1,2,3
10.	Floating Point Arithmetic	45m	PPT	1,2,3
11.	Modified booth's Algorithm	45m	PPT	1,2,3
12.	Revision	45m	PPT	-

LESSON PLAN

Sub Code & Name: **U14EC628 & WIRELESS COMMUNICATION**

Unit : III **Branch : ECE** **Semester: VII**

Session No.	Topics to be covered	Duration in Mins	Teaching Method	Books Ref
1.	Hardwired Control	45m	PPT	1,3,5
2.	Micro programmed Control	45m	PPT	1,2,3
3.	Multiplier Control Unit	45m	PPT	1,2
4.	CPU Control Unit	45m	PPT	1,2,3
5.	Pipeline Control	45m	PPT	1,2,3
6.	Instruction Pipelines	45m	PPT	1,2,4
7.	Arithmetic Pipelines	45m	PPT	1,2
8.	Superscalar Processing	45m	PPT	1,2
9.	Parallel processing	45m	PPT	1,2,3
10.	Revision	45m	PPT	1,2,3

	LESSON PLAN	
	Sub Code & Name: U15ECE31 & COMPUTER ARCHITECTURE **Unit : IV** **Branch : ECE** **Semester: V**	

Session No.	Topics to be covered	Duration in Mins	Teaching Method	Books Ref
1.	Basic concept of Semiconductor	45m	PPT	1,3,5
2.	Random Access Memories	45m	PPT	1,2,3
3.	Serial -Access Memories	45m	PPT	1,2
4.	RAM Interfaces	45m	PPT	1,2,3
5.	Magnetic Surface Recording	45m	PPT	1,2,3
6.	Magnetic Surface Recording	45m	PPT	1,2,4
7.	multilevel memories	45m	PPT	1,2
8.	Cache Memory	45m	PPT	1,2
9.	Virtual Memory	45m	PPT	1,2,3
10.	Memory Allocation	45m	PPT	1,2,3
11.	Associative Memory	45m	PPT	1,2,3
12.	Revision	45m	PPT	-

LESSON PLAN

Sub Code & Name: U15ECE31 & COMPUTER ARCHITECTURE

Unit : V **Branch : ECE** **Semester: V**

Session No.	Topics to be covered	Duration in Mins	Teaching Method	Books Ref
1.	Array Processors	45m	PPT	1,3,5
2.	Interconnection Structures	45m	PPT	1,2,3
3.	Inter processor Arbitration	45m	PPT	1,2
4.	Inter Processor Communication	45m	PPT	1,2,3
5.	Inter Processor Synchronization	45m	PPT	1,2,3
6.	Cache Coherence	45m	SEMINAR	1,2,4
7.	Shared Memory	45m	SEMINAR	1,2
8.	Multiprocessors	45m	SEMINAR	1,2
9.	RISC and CISC processors	45m	SEMINAR	1,2,3
10.	Superscalar processor	45m	SEMINAR	1,2,3
11.	vector processor	45m	SEMINAR	1,2,3
12.	Revision	45m	PPT	-

TEXTBOOK:

1. John P.Hayes, 'Computer architecture and Organization', 3rd Edition Tata McGraw-Hill.
2. V.Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organization", 5th Edition, McGraw-Hill Inc.
3. Computer Architecture a quantitative approach, John L. Hennessy and David A. Patterson, 4th Edition Elsevier.

FURTHER READINGS:

4. Morris Mano, "Computer System Architecture", 3rd Edition Prentice-Hall of India.
5. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition PHI/Pearson.
6. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson / PHI.
7. G.Kane & J.Heinrich, ' MIPS RISC Architecture ', Englewood cliffs, New Jersey, 4th Edition Prentice Hall.

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