	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2013-2014 onwards)					

SEMESTER – I								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13MA102	Applied Mathematics	3	1	0	4	50	50	100
P13VD101	Solid State Device Modeling and Simulation	3	1	0	4	50	50	100
P13VD102	VLSI Technology	3	0	0	3	50	50	100
P13VD103	VLSI Design Techniques	3	0	0	3	50	50	100
P13AE102	Advanced Digital System Design	3	0	0	3	50	50	100
P13VD104	DSP Integrated Circuits	3	0	0	3	50	50	100
PRACTICAL								
P13VD105	VLSI Design Lab I	0	0	3	2	50	50	100
		Total Credits			**22**	**350**	**350**	**700**

CA - Continuous Assessment, ESE - End Semester Examination

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Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**

CURRICULUM

(Applicable to the students admitted from the academic year 2013-2014 onwards)

SEMESTER – II								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13AE204	Analysis and Design of Analog Integrated Circuits	3	0	0	3	50	50	100
P13VD206	CAD for VLSI Circuits	3	0	0	3	50	50	100
P13VD207	Low Power VLSI Design	3	0	0	3	50	50	100
P13VD208	VLSI Signal Processing	3	0	0	3	50	50	100
	Elective-I	3	0	0	3	50	50	100
	Elective-II	3	0	0	3	50	50	100
PRACTICAL								
P13VD209	VLSI Design Lab II	0	0	3	2	50	50	100
		Total Credits			**20**	**350**	**350**	**700**

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CURRICULUM (Applicable to the students admitted from the academic year 2013-2014 onwards)					

SEMESTER – III								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
	Elective-III	3	0	0	3	50	50	100
	Elective-IV	3	0	0	3	50	50	100
	Elective-V	3	0	0	3	50	50	100
PRACTICAL								
P13VD310	Project Work(Phase I)	0	0	12	6	50	50	100
		Total Credits			**15**	**200**	**200**	**400**

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2013-2014 onwards)					

SEMESTER – IV								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
PRACTICAL								
P13VD411	Project Work(Phase II)	0	0	24	12	50	50	100
		Total Credits			**12**	**50**	**50**	**800**

CA - Continuous Assessment, ESE - End Semester Examination

LIST OF ELECTIVES								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P13VDE01	Testing of VLSI Circuits	3	0	0	3	50	50	100
P13VDE02	Analog VLSI Design	3	0	0	3	50	50	100
P13VDE03	Design of Semiconductor Memories	3	0	0	3	50	50	100
P13VDE04	Physical Design of VLSI Circuits	3	0	0	3	50	50	100
P13CSE18	Genetic Algorithms and their Applications	3	0	0	3	50	50	100
P13VDE05	ASIC Design	3	0	0	3	50	50	100
P13CSE19	Digital Speech Signal Processing	3	0	0	3	50	50	100
P13VDE06	DSP Processor Architecture and Programming	3	0	0	3	50	50	100
P13VDE07	Introduction to MEMS System Design	3	0	0	3	50	50	100
P13VDE08	System on Chip Design	3	0	0	3	50	50	100
P13AE101	Advanced Microprocessors and Microcontrollers	3	0	0	3	50	50	100
P13CSE16	Neural Networks and Its Applications	3	0	0	3	50	50	100
P13AEE04	Reliability Engineering	3	0	0	3	50	50	100
P13AEE05	Electromagnetic Interference and Compatibility in System Design	3	0	0	3	50	50	100
P13CSE08	Computer Architecture and Parallel Processing	3	0	0	3	50	50	100
P13AE207	Embedded Systems	3	0	0	3	50	50	100
P13AEE08	Nano Electronics	3	0	0	3	50	50	100

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**Common to VLSI , POWER SYSTEMS & APPLIED ELECTRONICS**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13MA102	**APPLIED MATHEMATICS**	3	0	0	3	50	50	100

Objectives	• At the end of the course Student would be exposed to fundamental knowledge in • One Dimensional random variables, Testing the hypothesis • Linear programming, Computational methods in Engineering and • Various Queuing models.		
Unit – I	**ONE DIMENSIONAL RANDOM VARIABLE**	Periods	**9+3**
Random Variables- Probability Function-Moments-Moment Generating Function & their Properties- Binomial, Poisson, Geometric, Uniform, Exponential Distributions:			
Unit – II	**TESTING OF HYPOTHESIS**	Periods	**9+3**
Basic Definitions:- (Population, Sampling, Tests of Significance, Testing a Hypothesis, Null Hypothesis, Alternative Hypothesis, Level of Significance, Types of Errors) – Testing of Hypothesis using : 't'-Test , 'F'-Test , Chi Square Test (ψ^2) - Test for Independence of Attributes & Goodness of Fit			
Unit – III	**LINEAR PROGRAMMING**	Periods	**9+3**
Formulation-Graphical solution-Simplex Method -Transportation and Assignment problems.			
Unit – IV	**DYNAMIC PROGRAMMING**	Periods	**9+3**
Dynamic Programming-principle of optimality-forward and backward recursion-DP Applications (Cargo loading method)-Problems of dimensionality.			
Unit – V	**QUEUING MODELS**	Periods	**9+3**

Introduction-Markovian Models: M/M/1**:** infinite capacity-M/M/C**:** infinite capacity-M/M/1**:** finite capacity – M/M/C**:** finite capacity, Little's formula.		
	Total Periods	**60**
REFERENCES:		
1.	B.V.Ramana – 'Higher Engineering Mathematics', by Tata Mc Graw Hill Publishing Pvt Ltd – New Delhi, 2008th Edition.	
2.	Taha,H.a., Operations Research: An Introduction,seventh Edition,Person Education edition,Asia,New Delhi(2002).	
3.	Moon,T.K.,Sterling,W.C.,Mathematical methods and algorithms for signal processing,Pearson Education,2000	
4.	Donald Gross and carl M.Harris, Fundamentals of queuing theory,2nd edition, john Wiley and Sons,New York(1985)	
5.	Richard Johnson,Miller&freund's probability and statistics for engineers,7th edition, Prentice-Hall of india,private Ltd.,New Delhi(2007)	

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN & APPLIED ELCETRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD101	**SOLID STATE DEVICE MODELING AND SIMULATION**	3	1	0	4	50	50	100

Objectives	• To study and model MOSFET and advanced MOSFET • To Model the Process Variation and quality assurance		
Unit- I	**MOSFET DEVICE PHYSICS**	Periods	**9**
MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.			
Unit -II	**NOISE MODELING**	Periods	**9**
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.			
Unit -III	**BSIMV4 MOSFET MODELING**	Periods	**9**

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitic model.			
Unit -IV	**OTHER MOSFET MODELS**	Periods	**9**
The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model.			
Unit- V	**MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE**	Periods	**9**
Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests.			
		Total Periods	**45**

REFERENCES:

1.	Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003.
2.	Christian C. Enz, Eric A. Vittoz, "Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design", John Wiley & Sons, Ltd, 2006.

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD102	**VLSI TECHNOLOGY**	3	0	0	3	50	50	100

Objectives	• To study the assembling packing techniques • To study about oxidation and lithography • To study about implantation		
Unit – I	**CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION**	Periods	**9**
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing, consideration, Vapor phase Epitaxy and Evaluation, Molecular Beam ,Silicon on Insulators, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.			
Unit – II	**LITHOGRAPHY AND RELATIVE PLASMA ETCHING**	Periods	**9**
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma, Dry Etching and Wet Etching and equipments.			
Unit – III	**DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION**	Periods	**9**

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation, Atomic Diffusion Mechanism , Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapor deposition – Patterning.			
Unit - IV	**PROCESS SIMULATION AND VLSI PROCESS INTEGRATION**	Periods	**9**
Ion implantation, Diffusion and oxidation, Epitaxy, Lithography, Etching and Deposition, NMOS IC Technology, CMOS IC Technology, MOS Memory IC technology ,IC Fabrication.			
Unit - V	**ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES**	Periods	**9**
Analytical Beams, Beams Specimen interactions, Chemical methods, Package type, banking design consideration, VLSI assembly technology, Package fabrication technology.			
		Total Periods	**45**
REFERENCES:			
1.	S.M.Sze, "VLSI Technology", McGraw-Hill Second Edition. 2002.		
2.	Douglas A. Puck ell and Kamran Eshraghian, " Basic VLSI Design", Prentice HallIndia. 2003.		
FURTHER READINGS:			
1.	Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000		

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Department	**VLSI DESIGN & APPLIED ELCETRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD103	**VLSI DESIGN TECHNIQUES**	3	0	0	3	50	50	100

Objectives	• To Understand the concepts of NMOS and PMOS transistors • To Understand the Basic CMOS technology • To Study the Multiplexers • To understand the concepts of Basics of CMOS testing. • To Understand the concepts of digital design with Verilog HDL		
Unit – I	**MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY**	Periods	**9**
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.			
Unit – II	**INVERTERS AND LOGIC GATES**	Periods	**9**
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.			

Unit – III	**CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION**	Periods	**9**
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.			
Unit – IV	**VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN**	Periods	**9**
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.			
Unit – V	**VERILOG HARDWARE DESCRIPTION LANGUAGE**	Periods	**9**
Overview of digital design with Verilog HDL, hierarchical modelling concepts, modules and port definitions, gate level modelling, data flow modelling, behavioral modelling, task & functions, Test Bench.			
		Total Periods	**45**

REFERENCES:

1.	Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2.	John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
3.	Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4.	Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS &VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE102	**ADVANCED DIGITAL SYSTEM DESIGN**	3	0	0	3	50	50	100

Objectives	• To provide an in-depth knowledge of synchronous and asynchronous sequential circuits analysis and design • To provide the basics of fault diagnosis and testing algorithms • To study the design of synchronous sequential circuits using PLDs • To study the design of digital systems using VHDL

Unit – I	**SEQUENTIAL CIRCUIT DESIGN**	Periods	**9**
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits -design of iterative circuits-ASM chart and realization using ASM			
Unit – II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	Periods	**9**
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.			
Unit – III	**FAULT DIAGNOSIS AND TESTABILITY**	Periods	**9**

	ALGORITHMS		
Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test			
Unit – IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**	Periods	**9**
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000			
Unit – V	**SYSTEM DESIGN USING VHDL**	Periods	**9**
VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier-Divider – Design of simple microprocessor.			
		Total Periods	**45**

REFERENCE:

1.	Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004

FURTHER READINGS:

1.	Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
2.	Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
3.	Parag K.Lala “Digital system Design using PLD” B S Publications,2003
4.	Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004
5.	Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill – 2006

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Department	**VLSI DESIGN &APPLIED ELCETRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD104	**DSP INTEGRATED CIRCUITS**	3	1	0	4	50	50	100

Objectives	• To study the advanced digital signal processors and IC technologies. • To explore the concepts of multi rate signal processing and multi rate filters. • To study the complex multipliers and VLSI layouts.		
Unit – I	**DSP INTEGARTED CIRCUITS & VLSI CIRCUIT TECHNOLOGIES**	Periods	**9**
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.			
Unit – II	**DIGITAL SIGNAL PROCESSING**	Periods	**9**
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.			
Unit – III	**DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**	Periods	**9**
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.			
Unit – IV	**DSP ARCHITECTURES & SYNTHESIS OF DSP ARCHITECTURES**	Periods	**9**
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.			
Unit – V	**SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS**	Periods	**9**
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. CORDIC algorithm.			
		Total Periods	**45**
REFERENCES:			
1.	Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York 1999		

2.	Oppenheim A.V. et.al, 'Discrete-time Signal Processing' Pearson education,2000
FURTHER READINGS:	
1.	Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second edition, Pearson education, Asia 2001
2.	Keshab K.Parhi, 'VLSI digital Signal Processing Systems design and Implementation' John Wiley & Sons, 1999

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD105	**VLSI DESIGN LAB I**	0	0	3	2	50	50	100

Objectives	• Design a sequential circuit using HDL. • Implementation of ALU and MAC in FPGA • Circuit simulation using PSICE • Implementation of DSP Algorithms

LIST OF EXPERIMENTS:

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using VERILOG.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE
5. Modeling of MOSFET using C.
6. Implementation of FFT, Digital Filters in DSP Processor.
7. Implementation of DSP algorithms using software package.
8. Implementation of MAC Unit using FPGA.

TOTAL PERIODS:60 HOURS

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Department	**APPLIED ELECTRONICS & VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE204	**ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS**	3	0	0	3	50	50	100

Objectives	• To provide an in-depth knowledge in computer fundamentals. • To provide the basics of C programming language. • To enhance the fundamental Application relevant to C programming language.		
Unit – I	**MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES**	Periods	**9**
Depletion region of PN junction– Large signal behavior of Bipolar Transistors–small signal model of bipolar transistors – large signal behavior of MOSFET – small signal of MOS transistors – short channel effects in MOS transistors– Weak inversion in MOS transistors – substrate current flow in MOS transistor.			
Unit – II	**CIRCUIT CONFIGURATION FOR LINEAR IC**	Periods	**9**
Current sources, Analysis of differential amplifiers with active load using BJT and FET, supply and temperature independent biasing technique, voltage references, output stages: current follower, source follower and push pull output stages.			
Unit – III	**OPERATIONAL AMPLIFIERS**	Periods	**9**
Analysis of operational amplifier circuit, slew rate model and high frequency analysis ,frequency response of integrated circuits: single stage and multistage amplifier and operational amplifiers noise.			
Unit – IV	**ANALOG MULTIPLIER AND PLL**	Periods	**9**
Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL-monolithic PLL design in integrated circuits: Sources of noise-noise model of integrated circuit components-circuit noise calculations-equivalent noise input generators-noise bandwidth-noise figure and noise temperature.			
Unit – V	**ANALOG DESIGN WITH MOS TECHNOLOGY**	Periods	**9**
Mos current mirrors-simple,c ascade, Wilson and widlar current sources-CMOS class AB output stages-two stage MOS operational amplifiers, with cascade, telescopic-cascode operational amplifiers-MOS folded cascade and MOS active cascade operational amplifiers.			
		Total Periods	**45**

REFERENCES:

1.	Gray, Meyer, Lewis and Hurst, "Analysis and design of analog ICs",Fourth Edition, Willey International,2002
2.	Behzad Razavi,"Principles of data conversion system design",S.Chand and company ltd,2000

FURTHER READINGS:

1.	Nandita Dasgupta,Amitava Dasgupta,"Semiconductor devices ,modeling and technology ", Prentice Hall of India Pvt Ltd,2004
2.	Grebene,Bipolar and MOS Analog Integrated ciruit design", John Wiley and sons.Inc.2003
3.	Phillip.E.Allen Douglas R Holberg ,CMOS Analog Integrated circuit design", second edition – Oxford University Press.2003

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD206	**CAD FOR VLSI CIRCUITS**	3	0	0	3	50	50	100

Objectives	• To provide an in-depth knowledge in VLSI Design methodology • Enhance the fundamentals of different data structures. • To Analysis different types of floor planning, placement and routing algorithms.		
Unit – I	**VLSI DESIGN METHODOLOGIES**	Periods	**9**
Introduction to VLSI Design methodologies - Review of Data structures and algorithms -Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.			
Unit – II	**DESIGN RULES**	Periods	**9**
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.			
Unit – III	**FLOOR PLANNING**	Periods	**9**
Floor planning concepts - shape functions and Floor plan sizing - Types of local Routing problems - Area routing - channel routing - global routing - algorithms for global routing.			
Unit – IV	**SIMULATION**	Periods	**9**
Simulation - Gate-level modelling and simulation - Switch-level modelling and simulation- Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.			
Unit – V	**MODELLING AND SYNTHESIS**	Periods	**9**
High level Synthesis - Hardware models - Internal representation - Allocation -assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.			
		Total Periods	**45**

REFERENCE:

1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002

FURTHER READING:

1.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution, Affiliated to Anna University ,Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD207	**LOW POWER VLSI DESIGN**	3	0	0	3	50	50	100

Objectives	• To study the principle of low power design. • To explore the concept of power optimization and estimation analysis. • To understand the layout design and special techniques. • To study the software design for low power techniques.		
Unit – I	**POWER DISSIPATION IN CMOS**	Periods	**9**
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.			
Unit – II	**POWER OPTIMIZATION**	Periods	**9**
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.			
Unit – III	**DESIGN OF LOW POWER CMOS CIRCUITS**	Periods	**9**
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.			
Unit – IV	**POWER ESTIMATION**	Periods	**9**
Power estimation techniques – Logic level power estimation – Simulation power analysis– Probabilistic power analysis.			
Unit – V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER**	Periods	**9**
Synthesis for low power –Behavioral level transforms- Software design for low power.			
		Total Periods	**45**

REFERENCES:

1.	K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002
3.	J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4.	A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5.	Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6.	Abdellatif Bellaouar, Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7.	James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD208	**VLSI SIGNAL PROCESSING**	3	0	0	3	50	50	100

Objectives	• To study the DSP Systems, Pipelining and Parallel processing of FIR Filters. • To understand the concept of Retiming, Algorithmic strength reduction. • To explore the Fast Convolution, Pipelining and Parallel Processing of IIR Filters. • To understand Scaling, Round-Off Noise, Bit-Level Arithmetic Architectures and Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining.

Unit – I	**INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**	Periods	**9**

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

Unit – II	**RETIMING, ALGORITHMIC STRENGTH REDUCTION**	Periods	**9**

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

Unit – III	**FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**	Periods	**9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

Unit – IV	**SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES**	Periods	**9**

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

Unit – V	**NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING**	Periods	**9**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining.Asynchronous pipelining bundled data versus dual rail protocol.

	Total Periods	**45**
REFERENCES:		
1.	Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and Implementation ", Wiley, Interscience, 2007.	
2.	U. Meyer – Baese, " Digital Signal Processing with Field Programmable GateArrays", Springer, Second Edition, 2004.	

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VD209	**VLSI DESIGN LAB II**	0	0	3	2	50	50	100

Objectives	• To Implementation of 8 Bit ALU in FPGA / CPLD. • To Implementation of 4 Bit Sliced processor in FPGA / CPLD. • To Implementation of Alarm clock controller using embedded microcontroller. • To Implementation of Alarm clock controller using embedded microcontroller .

LIST OF EXPERIMENTS:

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.

TOTAL PERIODS: 60 HOURS

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE01	**TESTING OF VLSI CIRCUITS**	3	0	0	3	50	50	100

Objectives	• To study the fault modelling and detection techniques. • To understand the test generation for combinationaland sequential logic circuits. • To explore the design for testsbility and self test methods. • To study the fault diagnosis.		
Unit – I	**BASICS OF TESTING AND FAULT MODELLING**	Periods	**9**
Introduction to testing – Faults in Digital Circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.			
Unit – II	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**	Periods	**9**
Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.			
Unit - III	**DESIGN FOR TESTABILITY**	Periods	**9**
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.			
Unit - IV	**SELF TEST AND TEST ALGORITHNS**	Periods	**9**
Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures– Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.			
Unit - V	**FAULT DIAGNOSIS**	Periods	**9**
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.			
		Total Periods	**45**

REFERENCES:

1.	M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
2.	P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

FURTHER READINGS:

1.	M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
2.	A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE02	**ANALOG VLSI DESIGN**	3	0	0	3	50	50	100

Objectives	• To study the basic CMOS & BICMOS circuit techniques in VLSI signal processing. • To understand the concept of A/D Converters And Analog Integrated Sensors • To Design For Testability And Analog Vlsi Interconnects**.** • To understand the concepts of Statistical Modeling and Simulation, Aided Design and Analog and Mixed Analog Digital Layout.

Unit – I	**BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW- VOLTAGE SIGNAL PROCESSING**	Periods	**9**

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

Unit – II	**BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT - MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING**	Periods	**9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

Unit – III	**SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS**	Periods	**9**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched- Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters- Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma- Delta Modulators-Interpolative Modulators – Cascaded Architecture-Decimation Filters- Sensors-Sensor Interfaces.

Unit – IV	**DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS**	Periods	**9**

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

Unit - V	**STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER- AIDED DESIGN AND ANALOG AND MIXED ANALOG DIGITAL LAYOUT**	Periods	**9**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

		Total Periods	**45**
REFERENCES:			
1.	Mohammed Ismail, Terri Fief, “Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994		
2.	Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS ",PrenticeHall, 1998		
3.	Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990		
4.	Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994		

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE03	**DESIGN OF SEMICONDUCTOR MEMORIES**	3	0	0	3	50	50	100

Objectives	• To understand different types of Volatile and Nonvolatile memories • To study memory fault modeling. • To study the radiation effects and packing Technologies.		
Unit - I	**RANDOM ACCESS MEMORY TECHNOLOGIES**	Periods	**9**
Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application,Specific DRAMs.			
Unit - II	**NONVOLATILE MEMORIES**	Periods	**9**
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.			
Unit - III	**MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE**	Periods	**9**
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.			
Unit - IV	**RELIABILITY AND RADIATION EFFECTS**	Periods	**9**
General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability- Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.			
Unit - V	**PACKAGING TECHNOLOGIES**	Periods	**9**
Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics- Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.			
		Total Periods	**45**
REFERENCES:			

1.	Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2.	Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3.	Betty Prince, “ Emerging Memories: Technologies and Trends”, Kluwer Academic Publishers, 2002

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE04	**PHYSICAL DESIGN OF VLSI CIRCUITS**	3	0	0	3	50	50	100

Objectives	• To study the VLSI technologies • To study placement routing, partitioning. • To study about floor planning and packing		
Unit - I	**INTRODUCTION TO VLSI TECHNOLOGY**	Periods	**9**
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies, Packaging-Computational Complexity-Algorithmic Paradigms			
Unit - II	**PLACEMENT USING TOP-DOWN APPROACH**	Periods	**9**
Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic, Ratiocut- partition with capacity and i/o constraints Floor planning, Rectangular dual floor planning, hierarchial approach- simulated annealing- Floor plan sizing, placement by simulated annealing partitioning placement- module placement on a resistive network – regular and linear placement.			
Unit - III	**ROUTING USING TOP DOWN APPROACH**	Periods	**9**
Maze Running- line searching- Steiner trees, Global Routing: Sequential Approaches- hierarchical approaches ulticommodity flow based techniques, Randomised Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based PGAs			
Unit - IV	**PERFORMANCE ISSUES IN CIRCUIT LAYOUT**	Periods	**9**
Delay Models- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.			
Unit - V	**SINGLE LAYER ROUTING,CELL GENERATION AND COMPACTION**	Periods	**9**
Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend inimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.			
		Total Periods	**45**
REFERENCES:			
1.	Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill		

	International Edition 1995
2.	Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE18	**GENETIC ALGORITHMS AND THEIR APPLICATIONS**	3	0	0	3	50	50	100

Objectives	• To study the assembling packing techniques • To study about oxidation and lithography • To study about implantation.		
Unit - I	**INTRODUCTION**	Periods	**9**
Introduction, GA Technology-Steady State Algorithm, Fitness Scaling-Inversion.			
Unit - II	**PARTITIONING AND PLACEMENT**	Periods	**9**
GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation, Partitioning algorithm Taxonomy Multiway Partitioning.			
Unit - III	**GENETICS**	Periods	**9**
Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas, Standard cell placement-GASP Algorithm-unified algorithm.			
Unit - IV	**ROUTING AND TEST PATTERN GENERATION**	Periods	**9**
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.			
Unit - V	**APPLICATIONS OF GENETICS**	Periods	**9**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.		
	Total Periods	**45**
REFERENCES:		
1.	Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall, 1998...	
2.	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley –Interscience, 1977.	
FURTHER READINGS:		
1.	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic.	
2.	John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition, May 1999.	

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**VLSI DESIGN& APPLIRD ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE05	**ASIC DESIGN**	3	0	0	3	50	50	100

Objectives	• To study about ASIC fundamentals. • To study different level of ASIC flow in detail. • To explore modeling of ASIC design.		
Unit - I	**INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN**	Periods	**9**
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.			
Unit - II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	Periods	**9**
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.			
Unit - III	**PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY**	Periods	**9**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation.			
Unit - IV	**LOGIC SYNTHESIS, SIMULATION AND TESTING**	Periods	**9**
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.			
Unit - V	**ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING**	Periods	**9**
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.			
		Total Periods	**45**

REFERENCES:

1.	M.J.S .Smith, “Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.
2.	Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991

3.	S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4.	Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5.	S. Y. Kung, H. J. Whilo House, T. Kailath, “VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6.	Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE19	**DIGITAL SPEECH SIGNAL PROCESSING**	3	0	0	3	50	50	100

Objectives	• To understand Speech generation and its properties • To analyze the speech signal in time and frequency domain. • To know about the application of speech signal.		
Unit - I	**MECHANICS OF SPEECH**	Periods	**9**
Speech production mechanism – Nature of Speech signal – Discrete time modeling of Speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulators features. Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics.			
Unit - II	**TIME DOMAIN METHODS FOR SPEECH PROCESSING**	Periods	**9**
Time domain parameters of Speech signal – Methods for extracting the parameters Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function.			
Unit - III	**FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING**	Periods	**9**
Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder— Channel Vocoder.			
Unit - IV	**LINEAR PREDICTIVE ANALYSIS OF SPEECH**	Periods	**9**
Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.			
Unit - V	**APPLICATION OF SPEECH SIGNAL PROCESSING**	Periods	**9**
Algorithms: Spectral Estimation, dynamic time warping, hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition –Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification– Voice response system – Speech Synthesis: Text to speech, voice over IP.			
		Total Periods	**45**

REFERENCES:

1.	Ben Gold and Nelson Morgan, Speech and Audio Signal Processing, John Wiley and Sons Inc. , Singapore, 2004
2.	L.R.Rabiner and R.W.Schaffer – Digital Processing of Speech signals – Prentice Hall-1978

3.	Quatieri – Discrete-time Speech Signal Processing – Prentice Hall – 2001
4.	J.L.Flanagan – Speech analysis: Synthesis and Perception – 2nd edition – Berlin –1972
5.	I.H.Witten – Principles of Computer Speech – Academic Press – 1982

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE06	**DSP PROCESSOR ARCHITECTURE AND PROGRAMMING**	3	0	0	3	50	50	100

Objectives	• To study fundamentals of Programmable DSPs • To study TMS processors and its applications • To learn about ADSP processors • To study advanced DSP Processors from Texas and Motorola.		
Unit - I	**FUNDAMENTALS OF PROGRAMMABLE DSPs**	Periods	**9**
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P- DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining –Special Addressing modes in P-DSPs – On chip Peripherals.			
Unit - II	**TMS320C5X PROCESSOR**	Periods	**9**
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.			
Unit - III	**TMS320C3X PROCESSOR**	Periods	**9**
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.			
Unit - IV	**ADSP PROCESSORS**	Periods	**9**
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.			
Unit - V	**ADVANCED PROCESSORS**	Periods	**9**
Architecture of TMS320C54X: Pipe line operation, Code Composer studio - Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.			
		Total Periods	**45**

REFERENCES:

1.	B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
2.	User guides Texas Instrumentation, Analog Devices, and Motorola.

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN/ ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE07	**INTRODUCTION TO MEMS SYSTEM DESIGN**	3	0	0	3	50	50	100

Objectives	• To study fundamentals of MEMS • To study Mechanics for MEMS Design • To study the design issues of MEMS • To study the principle of Optical and RF MEMS		
Unit - I	**INTRODUCTION TO MEMS**	Periods	**9**
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelorometers and Micro fluidics, MEMS materials, Micro fabrication			
Unit - II	**MECHANICS FOR MEMS DESIGN**	Periods	**9**
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.			
Unit - III	**ELECTRO STATIC DESIGN**	Periods	**9**
Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.			
Unit - IV	**CIRCUIT AND SYSTEM ISSUES**	Periods	**9**
Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.			
Unit - V	**INTRODUCTION TO OPTICAL AND RF MEMS**	Periods	**9**
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.			
		Total Periods	**45**

REFERENCES:

1.	Stephen Santuria," Microsystems Design", Kluwer publishers, 2000
2.	Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
3.	Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000
4.	Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2013**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13VDE08	**SYSTEM ON CHIP DESIGN**	3	0	0	3	50	50	100

Objectives	• To understand the concepts of System on Chip Design methodology for Logic and Analog Cores. • To understand the concepts of System on Chip Design Validation. • To understand the concepts of SOC Testing.		
Unit - I	**INTRODUCTION**	Periods	**9**
System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.			
Unit - II	**DESIGN METHODOLOGICAL FOR LOGIC CORES**	Periods	**9**
SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores –Designing with hard cores, soft cores- Core and SoC design examples.			
Unit - III	**DESIGN METHODOLOGY FOR MEMORY AND ANALOG CORES**	Periods	**9**
Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase- located loops –High I/O.			
Unit - IV	**DESIGN VALIDATION**	Periods	**9**
Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification.Case Study: Validation and test of systems on chip.			
Unit - V	**SOC TESTING**	Periods	**9**
SoC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories. Case Study: Integrating BIST techniques for on-line SoC testing.			
		Total Periods	**45**

REFERENCES:

1.	Rochit Rajsunah, System-on-a-chip: Design and Test, Artech House, 2007.
2.	Prakash Raslinkar, Peter Paterson & Leena Singh, System-on-a-chip verification: Methodology and Techniques, Kluwer Academic Publishers, 2000.
3.	M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems, Springer, 2007.
4.	L.Balado, E. Lupon, Validation and test of systems on chip, IEEE conference on SIC/SOC,1999.
5.	A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing, 2005.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE101	**ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS**	3	0	0	3	50	50	100

Objectives	• To introduce the concepts of advanced microprocessors. • To provide an in-depth knowledge about microprocessor architecture • To familiarize the basic architecture of Pentium family of processors. • To know about the inner workings of the 68HC11 microprocessor • To understand the essentials of PIC microcontrollers design and programming using assembly language.		
Unit - I	**MICROPROCESSOR ARCHITECTURE**	Periods	**9**
Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline– pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.			
Unit - II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM**	Periods	**9**
CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.			
Unit - III	**HIGH PERFORMANCE RISC ARCHITECTURE – ARM**	Periods	**9**
Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor**.**			
Unit - IV	**MOTOROLA 68HC11 MICROCONTROLLERS**	Periods	**9**
Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.			
Unit - V	**PIC MICROCONTROLLER**	Periods	**9**
CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers**.**			
		Total Periods	**45**

REFERENCES:

1.	Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2.	James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education ,1997.

FURTHER READINGS:

1.	Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
2.	Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003. John.B.Peatman

3.	John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
4.	John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE16	**NEURAL NETWORKS AND ITS APPLICATIONS**	3	0	0	3	50	50	100

Objectives	• To study the basic network learning algorithms • To understand the concept of radial basis networks and functions • To study committee machines and aerodynamics systems • To study attractor neural networks and adaptive resonance theory • To understand the concept of self organizing maps and pulsed neuron models.

Unit - I	**BASIC LEARNING ALGORITHMS**	Periods	**9**

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feedforward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering-Beamforming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.

Unit - II	**RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES RADIAL BASIS FUNCTION NETWORKS**	Periods	**9**

Cover's Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification. Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - - insensitive Loss Function – Support Vector Machines for Nonlinear Regression.

Unit - III	**COMMITTEE MACHINES**	Periods	**9**

Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model

NEURODYNAMICS SYSTEMS:

Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems- Lyapunov Stability – Neurodynamical Systems – The Cohen-Grossberg Theorem.

Unit - IV	**ATTRACTOR NEURAL NETWORKS**	Periods	**9**

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications

ADAPTIVE RESONANCE THEORY:

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center – Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications

Unit - V	**SELF ORGANISING MAPS**	Periods	**9**

Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications

PULSED NEURON MODELS:

Spiking Neuron Model – Integrate-and-Fire Neurons – Conductance Based Models – Computing with Spiking Neurons.

	Total Periods	**45**

REFERENCES:

1.	Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2.	Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3.	Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.
4.	James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE04	**RELIABILITY ENGINEERING**	3	0	0	3	50	50	100

Objectives	• Apply engineering knowledge to prevent or reduce frequency of failures • Identify and correct the causes of the failures • Define methods to mitigate the failures that occur if their causes have not been corrected • Apply techniques to estimate the reliability of new designs and analyze reliability data		
Unit - I	**PROBABILITY PLOTTING AND LOAD-STRENGTH**	Periods	**9**
Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.			
Unit - II	**RELIABILITY PREDICTION, MODELLING AND DESIGN**	Periods	**9**
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis			
Unit - III	**ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY**	Periods	**9**
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.			
Unit - IV	**RELIABILITY TESTING AND ANALYSIS**	Periods	9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.			
Unit - V	**MANUFACTURE AND RELIABILITY MAQNAGEMENT**	Periods	9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.			
		Total Periods	**45**

REFERENCES:

1.	Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002

2.	David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3.	Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE E05	**ELECTROMAGNETICINTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**	3	0	0	3	50	50	100

Objectives	• To study the Electromagnetic Interference concepts, coupling principles and Control Techniques • To design PCB for Electromagnetic compatability • To study instruments and measurements for Electromagnetic Interference		
Unit - I	**EMI/EMC CONCEPTS**	Periods	**9**
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.			
Unit - II	**EMI COUPLING PRINCIPLES**	Periods	**9**
Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.			
Unit - III	**EMI CONTROL TECHNIQUES**	Periods	**9**
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.			
Unit - IV	**EMC DESIGN OF PCBS**	Periods	**9**
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.			
Unit - V	**EMI MEASUREMENTS AND STANDARDS**	Periods	**9**
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.			
		Total Periods	**45**

References:

1.	V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2.	Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3.	Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.
4.	C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992.
5.	Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**COMPUTER SCIENCE, VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13CSE08	**COMPUTER ARCHITECTURE AND PARALLEL PROCESSING**	3	0	0	3	50	50	100

Objective	• To Understand Computer Design and Architecture • To understand the state-of-the-art in parallel processing and computer hardware technologies		
Unit – I	**THEORY OF PARALLELISM**	Periods	**9**
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.			
Unit – II	**PARTITIONING AND SCHEDULING**	Periods	**9**
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.			
Unit – III	**HARDWARE TECHNOLOGIES**	Periods	**9**
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.			
Unit – IV	**PIPELINING AND SUPERSCALAR TECHNOLOGIES**	Periods	**9**
Parallel and scalable architectures, Multiprocessor and Multicomputer, Multivectorand SIMD computers, Scalable, Multithreaded and data flow architectures.			
Unit – V	**SOFTWARE AND PARALLEL PROGRAMMING**	Periods	**9**
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.			
		Total Periods	**45**

REFERENCES:

1.	Kai Hwang, “Advanced Computer Architecture ", McGraw Hill International, 2001.

FURTHER READINGS:

1.	Dezso Sima, Terence Fountain, Peter Kacsuk, ”Advanced Computer architecture – A design Space Approach” , Pearson Education , 2003.
2.	John P.Shen, “Modern processor design . Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
3.	John P.Shen, “Modern processor design . Fundamentals of super scalar processors”, Tata

	McGraw Hill 2003.
4.	Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, Tata Mc-Graw Hill, 5th Edition, , 2002.

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Programme	**M.E.**	Programme Code		Regulation	**2013**
Department	**APPLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AE207	**EMBEDDED SYSTEMS**	3	0	0	3	50	50	100

Objectives	• To provide an in-depth knowledge of embedded system. • To provide the basics of embedded processor. • To study the design of embedded processor and computing platform. • To study the design of networks.		
Unit - I	**EMBEDDED PROCESSORS**	Periods	**9**
Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description and Design Example: Model Train Controller, ARM processor processor and memory organization.			
Unit - II	**EMBEDDED PROCESSOR AND COMPUTING PLATFORM**	Periods	**9**
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture.			
Unit - III	**NETWORKS**	Periods	**9**
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.			
Unit - IV	**REAL-TIME CHARACTERISTICS**	Periods	**9**
Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.			
Unit - V	**SYSTEM DESIGN TECHNIQUES**	Periods	**9**
Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.			
		Total Periods	**45**
REFERENCES:			
1.	Wayne Wolf, “Computers as Components: Principles of Embedded Computing		

	System Design", Morgan Kaufman Publishers.
2.	Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia.
3.	C. M. Krishna and K. G. Shin, "Real-Time Systems" , McGraw-Hill, 1997
4.	Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P13AEE08	**NANO ELECTRONICS**	3	0	0	3	50	50	100

Objectives	• To acquire knowledge about fundamental quantum mechanics. • To study about architecture and operations of different nano structures. • To comprehend the low dimension, high speed and low power design techniques and methodologies.		
Unit - I	**TECHNOLOGY AND ANALYSIS**	Periods	**9**
Film Deposition Methods – Lithography- Material removing techniques - Etching and Chemical-Mechanical Polishing - Scanning Probe Techniques.			
Unit - II	**CARBON NANO STRUCTURES**	Periods	**9**
Carbon Clusters - Carbon Nano tubes – Fabrication – Electrical, Mechanical and Vibrational Properties – Applications of Carbon Nano tubes.			
Unit - III	**LOGIC DEVICES**	Periods	**9**
Silicon MOSFET's – Novel materials and alternative concepts – Ferroelectric Field Effect Transistors – Super conductor digital electronics – Carbon Nano tubes for data processing.			
Unit - IV	**RANDOM ACCESS MEMORIES AND MASS STORAGE DEVICES**	Periods	**9**
High Permittivity material for DRAM's – Ferro electric Random Access memories – Magneto- resistive RAM-Hard Disk Drives – Magneto Optical Disks – Rewriteable DVDs based on Phase Change Materials – Holographic Data Storage.			
Unit - V	**DATA TRANSMISSION AND INTERFACES AND DISPLAYS**	Periods	**9**
Photonic Networks – Microwave Communication System – Liquid Crystal Displays – Organic Light emitting diodes.			
		Total periods	**45**

REFERENCES:

1.	Rainer Waser, Nano Electronics and Technology, Wiley VCH, 2003.
2.	Charles Poole, Introduction to Nano Technology, Wiley Inter science, 2003.
3.	C.Wasshuber, Simon , Simulation of Nano Structures Computational Single-Electronics, Springer-Velag,2001.
4.	Rainer Waser, Nano Electronics and information technology advanced electronic materials and novel devices, Wiley –VcH Verlag GmBh-KgaH, Germany, 2005.
5.	A. Mark Reed and Takhee Lee, Molecular Nano Electronics, American Scientific Publisher, California,2003.