	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2014-2015 onwards)					

SEMESTER – I								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P14MA101	Applied Mathematics	3	1	0	4	50	50	100
P14VD101	VLSI Technology	3	0	0	3	50	50	100
P14VD102	VLSI Design	3	1	0	4	50	50	100
P14VD103	Solid State Devices	3	1	0	4	50	50	100
P14VD104	CMOS Analog VLSI Design	3	0	0	3	50	50	100
P14VD105	M.E. Seminar	3	0	0	3	50	50	100
PRACTICAL								
P14VD106	VLSI Laboratory I	0	0	3	2	50	50	100
		Total Credits			**23**	**350**	**350**	**700**

CA - Continuous Assessment, ESE - End Semester Examination

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2014-2015 onwards)					

SEMESTER – II								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P14VD207	Low Power VLSI Design	3	0	0	3	50	50	100
P14VD208	VLSI Signal Processing	3	0	0	3	50	50	100
P14VD209	ASIC Design	3	0	0	3	50	50	100
P14VD210	Foundations of VLSI CAD	3	0	0	3	50	50	100
	Elective - I	3	0	0	3	50	50	100
	Elective - II / R&D project with convener approval	3	0	0	3	50	50	100
PRACTICAL								
P14VD211	VLSI Laboratory II	0	0	3	2	50	50	100
		Total Credits			**20**	**350**	**350**	**700**

CA - Continuous Assessment, ESE - End Semester Examination

	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2014-2015 onwards)					

SEMESTER – III								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
	Elective - III	3	0	0	3	50	50	100
	Elective - IV	3	0	0	3	50	50	100
	Institute Elective / Elective -V	3	0	0	3	50	50	100
PRACTICAL								
P14VD312	Project Stage I	0	0	12	6	50	50	100
		Total Credits			**15**	**200**	**200**	**400**

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	VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN (Autonomous Institution Affiliated to Anna University Chennai) Elayampalayam, Tiruchengode – 637 205				
Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN /** **ELECTRONICS AND COMMUNICATION ENGINEERING**				
CURRICULUM (Applicable to the students admitted from the academic year 2014-2015 onwards)					

SEMESTER – IV								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
PRACTICAL								
P14VD413	Project Stage II	0	0	24	12	50	50	100
		Total Credits			**12**	**50**	**50**	**100**

CA - Continuous Assessment, ESE - End Semester Examination

*Project stage 2 is a continuation of project stage 1

LIST OF ELECTIVES								
Course Code	Course Name	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
THEORY								
P14VDE01	Physics of Nanoscale Devices 1	3	0	0	3	50	50	100
P14VDE02	Physics of Nanoscale Devices 2	3	0	0	3	50	50	100
P14VDE03	Design of Experiments / Taguchi Method for Research	3	0	0	3	50	50	100
P14VDE04	RF Microelectronics chip design	3	0	0	3	50	50	100
P14VDE05	Physics of MOS Transistors	3	0	0	3	50	50	100
P14VDE06	Simulation of Circuits and Devices	3	0	0	3	50	50	100
P14VDE07	System Design	3	0	0	3	50	50	100
P14VDE08	Introduction to MEMS	3	0	0	3	50	50	100
P14VDE09	Testing and Verification of VLSI circuits	3	0	0	3	50	50	100
P14VDE10	Advance Network Analysis	3	0	0	3	50	50	100
P14VDE11	Embedded System Design	3	0	0	3	50	50	100
P14VDE12	Mixed Signal VLSI Design	3	0	0	3	50	50	100

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Programme	**M.E.**	Programme Code		Regulation	**2014**
Department	**VLSI , POWER SYSTEMS AND APPLIED ELECTRONICS**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14MA101	**APPLIED MATHEMATICS**	3	1	0	4	50	50	100

Objectives	• At the end of the course Student would be exposed to fundamental knowledge in • One Dimensional random variables, Testing the hypothesis • Linear programming, Computational methods in Engineering and • Various Queuing models.

Random Variables- Probability Function-Moments-Moment Generating Function & their Properties- Binomial, Poisson, Geometric, Uniform, Exponential Distributions, Testing of Hypothesis**,** Basic Definitions:- (Population, Sampling, Tests of Significance, Testing a Hypothesis, Null Hypothesis, Alternative Hypothesis, Level of Significance, Types of Errors) – Testing of Hypothesis using : 't'-Test , 'F'-Test , Chi Square Test (ψ^2) - Test for Independence of Attributes & Goodness of Fit. Linear Programming, Formulation-Graphical solution-Simplex Method -Transportation and Assignment problems. Dynamic Programming-principle of optimality-forward and backward recursion-DP Applications (Cargo loading method)-Problems of dimensionality. Queuing Models**,** Introduction-Markovian Models: M/M/1**:** infinite capacity-M/M/C**:** infinite capacity-M/M/1**:** finite capacity – M/M/C**:** finite capacity, Little's formula.

	Total Periods	**60**

REFERENCES:

1.	B.V.Ramana – 'Higher Engineering Mathematics', by Tata McGraw Hill Publishing Pvt Ltd – New Delhi, 2008th Edition.
2.	Taha,H.a., Operations Research: An Introduction, seventh Edition, Person Education edition, Asia, New Delhi(2002).
3.	Moon,T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education,2000
4.	Donald Gross and Carl M.Harris, Fundamentals of queuing theory,2nd edition, john Wiley and Sons, New York(1985)
5.	Richard Johnson, Miller & Freund's. "Probability and statistics for engineers,7th edition, Prentice-Hall of India, Private Ltd., New Delhi(2007)

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD101	**VLSI TECHNOLOGY**	3	0	0	3	50	50	100

Objectives	• To study about estimation of power. • To study software design for low power

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation: Solid State diffusion modeling and technology, Ion Implantation modeling, technology and damage annealing, characterization of Impurity profiles. Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, Characterization of oxide films, High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation. Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Epitaxial growth of silicon, modelling and technology. Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnect Multi-level metallization schemes. Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits, Advanced MOS technologies.

	Total Periods	**45**

REFERENCES:

1.	C.Y. Chang and S.M.Sze (Ed),ULSI Technology, McGraw Hill Companies Inc, 1996
2.	S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983
3.	S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.

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Programme	**M.E.**	Programme Code		Regulation	**2014**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD102	**VLSI Design**	3	1	0	4	50	50	100

Objectives	• To Understand the concepts of NMOS and PMOS transistors • To Understand the Basic CMOS technology • To Study the Multiplexers • To understand the concepts of Basics of CMOS testing. • To Understand the concepts of digital design with Verilog HDL

Review of MOS transistor models. CMOS logic families including static, dynamic and dual rail logic. Integrated Circuit Layout: Design Rules, Parasitics. Building blocks: ALU's, FIFO's, counters. VLSI system design: data and control path design, floor planning, Design methodology: Introduction to hardware description languages (VHDL), logic, and circuit and layout verification. Design examples.

Total Periods	**60**

REFERENCES:

1.	N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985
2.	L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley, 1985
3.	C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979
4.	J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997

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Programme	**M.E.**	Programme Code		Regulation	**2014**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD103	**SOLID STATE DEVICES**	3	1	0	4	50	50	100

Objectives	• To study Fundamentals of physics • To study different level of flow in detail
Electrons in solids, Band theory, Charge carriers in semiconductors, Boltzmann Transport Equation, p-n junctions, Schottky and MIS contacts, Field-effect transistors, Bipolar transistors, Optoelectronic and photovoltaic devices.	
Total Periods	**60**

REFERENCES:

1.	Streetman and Banerjee, Solid State Electronic Devices, Prentice Hall, 6/e 2005
2.	Sze and Ng, Physics of Semiconductor Devices, Wiley-Interscience, 3/e 2006

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Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD104	**CMOS Analog VLSI Design**	3	0	0	3	50	50	100

Objectives	• To study Fundamentals of cascade circuits • To study Fundamentals Basic MOS models

Introduction to analog VLSI and mixed signal issues in CMOS technologies. Basic MOS models, SPICE Models and frequency dependent parameters. Basic MNOS/CMOS gain stage, cascade and cascode circuits. Frequency response, stability and noise issues in amplifiers. CMOS analog blocks: Current Sources and Voltage references. Differential amplifier and OPAMP design. Frequency Synthesizers and Phased lock-loop. Non-linear analog blocks: Comparators, Charge-pump circuits and Multipliers. Data converters. Analog Interconnects. Analog Testing and Layout issues. Low Voltage and Low Power Circuits. Introduction to RF Electronics. Basic concepts in RF design.

	Total Periods	**45**

REFERENCES:

1.	R.Jacob Baker,H.W.Li, and D.E. Boyce CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of ,1998
2.	Mohammed Ismail and Terri Faiz Analog VLSI Signal and Information Process, McGraw-Hill Book company,1994
3.	Paul R. Gray and R.G.Meyer, Analysis and design of Analog Integrated circuits John Wiley and sons,,(3rd Edition),1993
4.	B. Razavi, RF Microelectronics, Prentice-Hall PTR,1998
5.	Journals: 1) IEEE Journal of Solid state Circuits 2) IEEE Trans. on Communications

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Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**I**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD106	**VLSI LABORATORY I**	0	0	3	2	50	50	100

Objectives	• Design a sequential circuit using HDL. • Implementation of ALU and MAC in FPGA • Circuit simulation using PSICE • Implementation of DSP Algorithms

List of Experiments:

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using VERILOG.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE
5. Modeling of MOSFET using C.
6. Implementation of FFT, Digital Filters in DSP Processor.
7. Implementation of DSP algorithms using software package.
8. Implementation of MAC Unit using FPGA.

Total Periods: 45

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Programme	**M.E.**	Programme Code		Regulation	**2014**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD207	**Low Power VLSI Design**	3	0	0	3	50	50	100

Objectives	• To study the principle of low power design. • To explore the concept of power optimization and estimation analysis. • To understand the layout design and special techniques. • To study the software design for low power techniques.

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design. Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers– Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques Power estimation techniques – Logic level power estimation – Simulation power analysis– Probabilistic power analysis. Synthesis for low power –Behavioral level transforms- Software design for low power

Total Periods	**45**

REFERENCES:

1.	K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002
3.	J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4.	A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5.	Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6.	Abdellatif Bellaouar, Mohamed.I. Elmasry, Low power digital VLSI design" Kluwer, 1995.
7.	James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

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Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD208	**VLSI SIGNAL PROCESSING**	3	0	0	3	50	50	100

Objectives	• To study the DSP Systems, Pipelining and Parallel processing of FIR Filters. • To understand the concept of Retiming, Algorithmic strength reduction. • To explore the Fast Convolution, Pipelining and Parallel Processing of IIR Filters. • To understand Scaling, Round-Off Noise, Bit-Level Arithmetic Architectures and Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining.

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, Fast convolution Look-Ahead pipelining in first-order IIR filters Clustered look-ahead pipelining, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching.

	Total Periods	**45**

REFERENCES:

1.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2.	U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

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Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD209	**ASIC DESIGN**	3	0	0	3	50	50	100

Objectives	• To study about ASIC fundamentals • To study different level of ASIC flow in detail • To explore modeling of ASIC design

Introduction to ASIC, ASIC library design, Programmable ASICs, Programmable ASIC logic cells, I/O cells and interconnects, Programmable ASIC design software, low level design entry, logic synthesis, simulation, Test, ASIC construction. System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

Total Periods	**45**

REFERENCES:

1.	M.J.S .Smith, "Application - Specific Integrated Circuits" - Addison -Wesley Longman Inc., 1997.
2.	Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3.	S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5.	S. Y. Kung, H. J. Whilo House, T. Kailath, "VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6.	Jose E.France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD210	**FOUNDATIONS OF VLSI CAD**	3	0	0	3	50	50	100

Objectives	• To study about complementary orthogonality • To study different level linear equations and Graphs • To explore modeling of Data structures such as stacks

Matrices: Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces and solution spaces of linear equations; Graphs: representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit and cutset matrices; Voltage and current spaces of a directed graph and their complementary orthogonality; Algorithms and data structures: efficient representation of graphs; Elementary graph algorithms involving BFS and DFS trees, such as finding connected and 2- connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph; Data structures such as stacks, linked lists and queues, binary trees and heaps. Time and space complexity of algorithms.

	Total Periods	**45**

REFERENCES:

1.	K. Hoffman and R.E. Kunze, Linear Algebra, Prentice Hall (India), 1986
2.	T.Cormen, C.Leiserson and R.A.Rivest, Algorithms, MIT Press and McGraw-Hill, 1990

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	**II**

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VD211	**VLSI LABORATORY II**	0	0	3	2	50	50	100

Objectives	• Design a sequential circuit using HDL. • Implementation of ALU and MAC in FPGA • Circuit simulation using PSICE • Implementation of DSP Algorithms

List of Experiments:

Theory: Introduction to Unix; Circuit simulation using SPICE, application of SPICE for analog design. Timing simulation with IRSIM, Design of static and dynamic digital circuits with IRSIM. Layout of integrated circuits. Use of the layout tool MAGIC for analog and digital integrated circuits; Laboratory: Tutorials on UNIX and vi. Tutorials and design exercises on linear circuit design with SPICE; Tutorial and exercises on digital design and timing analysis using IRSIM; Tutorials and exercises on IC layout using MAGIC; Group projects on design, analysis and layout of integrated circuits.

Total Periods: 45

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Programme	**M.E.**	Programme Code		Regulation	**2014**
Department	**VLSI DESIGN & APPLIED ELECTRONICS / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE01	**PHYSICS OF NANO ELECTRONIC DEVICES I**	3	0	0	3	50	50	100

Objectives	• To study about atom, tunneling • To study different level Fermi-Dirac statistics • To explore modeling of scattering in semiconductors

Particles and waves, the time-independent Schrödinger equation, states and operators, particle-in-a-box, density-of-states, harmonic oscillator, hydrogen atom, tunneling, two-level systems; Electrons in a crystal lattice, quantum well, wire and dot devices, interacting quantum wells, scanning probe microscopy, excitons in semiconductors, spin-1/2 systems and quantum bits; Identical particles fermions and bosons, field quantization: phonons and photons; Classical and quantum density, entropy and information, statistical ensembles, Bose-Einstein and Fermi-Dirac statistics applications to electronic devices; Non-equilibrium statistical mechanics transition probabilities, the master equation, the Boltzmann Transport Equation for electrons in solids; Perturbation theory, scattering rates and lifetimes in electronic devices; honon scattering in semiconductors, absorption and emission of photons in semiconductors: lasers and solar cells.

	Total Periods	**45**

REFERENCES:

1.	Hagelstein, Senturia and Orlando, Introductory Applied Quantum and Statistical Mechanics, Wiley 2004.
2.	Griffiths, Introduction to Quantum Mechanics, Prentice Hall 1995
3.	Gershenfeld, The Physics of Information Technology, Cambridge University Press, 2000

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE02	**PHYSICS OF NANO ELECTRONIC DEVICES II**	3	0	0	3	50	50	100

Objective	• To study about atom, tunneling • To study different level Fermi-Dirac statistics • To explore modeling of scattering in semiconductors

Pre-requisties Physics of Nanoelectronic Devices Ior equivalent, undergraduate-level engineering mathematics linear algebra, differential equations, Fourier analysis (MA 106, MA108, MA205, MA207 or equivalent), engineering physics (PH103 or equivalent), and post-graduate level solid-state devices (EE661 or equivalent).;Atomic structure: crystal structure, defects in solids.; Electronic structure: energy bands in solids, electron-electron interactions, band structure calculations, band structure engineering, Mechanical properties: Phonon engineering, elasticity and strain engineering, Semi-classical transport properties: dynamics of Bloch electrons, Zener tunneling and its device applications, the Boltzmann Transport Equation and its moments, drift-diffusion, hydrodynamic equations and Monte-Carlo simulation of semiconductor devices, thermoelectric and magneto electric phenomena; Nanoscale transport properties: scattering formalism, ballistic nano-transistors, Greens functions, Feynman paths, quantum-interference devices.; Optical properties: Maxwell's equations in dielectric media, polarization in insulators, ferroelectrics, polarons and polaritons, direct and indirect transitions in semiconductors, excitons, optoelectronic and photovoltaic devices, frequency response of metals skin-depth, plasma frequency, plasmonic devices.; Magnetic properties: Diamagnetism and paramagnetism of ions and electrons, magnetic interactions and ferromagnetic ordering, mean field theory, symmetry-breaking and phase transitions, spintronic devices.

	Total Periods	**45**

REFERENCES:

1.	Hagelstein, Senturia and Orlando, Introductory Applied Quantum and Statistical Mechanics, Wiley 2004.
2.	Griffiths, Introduction to Quantum Mechanics, Prentice Hall 1995
3.	Gershenfeld, The Physics of Information Technology, Cambridge University Press, 2000

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Programme	**M.E.**	Programme Code	**205**	Regulation	**2014**
Department	**VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**			Semester	

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE03	**DESIGN OF EXPERIMENTS / TAGUCHI METHOD FOR RESEARCH**	3	0	0	3	50	50	100

Objective	• To study about Taguchi Method, • To study design of orthogonal array • To explore modeling packaging related wire and die

Fundamentals of classical statistical methods: Normal Probability distribution, Statistical analysis of Means and Variance, Evolution of Taguchi Methods; Fundamentals of Taguchi Methods: Basic philosophy of Taguchi loss function and robust design, 8-steps in Taguchi Method, P-diagrams of Static and Dynamic problems, Definitions of signal, noise and control factors, Degrees of freedom, Linear graphs and orthogonal arrays and their designs, Definitions of Signal to Noise ratio, Evaluation of sensitivity to noise, Resolution of design, Analysis of Means, Means Plots and Analysis of Variance, Prediction of optimum conditions, Prediction of error variance; Design of Experiments for Robust Design: Identification of signal, noise and control variables, Identification and selection interactions, Control factors and their levels, Strategies for experimentation using Taguchi methods, beginner, intermediate and advanced strategies, Selection of design of orthogonal array, Modification of orthogonal arrays and linear graphs, Performing matrix experiments, Methods of analyzing experimental data, Interpretation of results; Application Examples: Application of design of experiments for circuit design for temperature insensitivity, robust design of sensors with reduced cross-sensitivities, designing robust processes: machining and cutting tool wear analysis, surface quality optimization, metallurgical structure optimization, packaging related wire and die bonding optimization, Application of design of experiments for optimizing product performance and process yield.

	Total Periods	**45**

REFERENCES:

1.	M.S. Phadke, "Quality Engineering using Robust Design" Prentice Hall (1989)

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE04	**RF MICROELECTRONICS CHIP DESIGN**	3	0	0	3	50	50	100

Objective	• To study about Resonator-less VCO • To study VLSI implementation • To study of Linearization techniques

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion. Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation. Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonator-less VCO design. Quadrature and single-sideband generators, Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearization techniques, Design issues in integrated RF filters; Some discussion on available CAD tools for RF VLSI designs.

	Total Periods	**45**

REFERENCES:

1.	B.Razavi, RF Microelectronics, Prentice-Hall PTR,1998
2.	T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits", Press, 1998
3.	R.Jacob Baker,H.W.Li, and D.E. Boyce, CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of ,1998
4.	Y.P. Tsividis Mixed Analog and Digital VLSI Devices and Technology, McGraw Hill,1996

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE05	**PHYSICS OF MOS TRANSISTORS**	3	0	0	3	50	50	100

Objective	• To study about atom, tunneling • To study different level Fermi-Dirac statistics • To explore modeling of scattering in semiconductors

The MOS transistor: Pao-Sah and Brews models; Short channel effects in MOS transistors. Hot-carrier effects in MOS transistors; Quasi-static compact models of MOS transistors; Measurement of MOS transistor parameters; Scaling and transistors structures for ULSI; Silicon-on-insulator transistors; High-field and radiation effects in transistors; The bipolar transistor: Ebers-Moll model; charge control model; small-signal and switching characteristics; Graded-base and graded-emitter transistors; High-current and high-frequency effects; Heterojunction bipolar transistors; Junction FETs; JFET, MESFET and heterojunction FET.

Total Periods	**45**

REFERENCES:

1.	N. D. Arora, MOSFET Models for VLSI Circuit Simulation, Springer-Verlag, 1993.
2.	E. J. Roulston, Bipolar Semiconductor Devices, McGraw-Hill, 1990
3.	S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
4.	Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
5.	E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE06	**SIMULATION OF CIRCUITS AND DEVICES**	3	0	0	3	50	50	100

Objective	• To study Formulation of network equations • To explore semiconductor parameters

Formulation of network equations: Nodal, mesh, modified nodal and hybrid analysis equations; Sparse matrix techniques; Solution of nonlinear networks through Newton-Raphson technique; Multistep methods: convergence and stability; Special classes of multistep methods: Adams-bash forth, Adams-Moulton and Gear's methods; Solution of stiff systems of equations; Adaptation of multistep methods to the solution of electrical networks; General purpose circuit simulators; Review of semiconductor equations (Poisson, continuity, drift-diffusion, trap rate). Finite difference formulation of these equations in 1D and 2D. Grid generation; Physical/empirical models of semiconductor parameters (mobility, lifetime, band gap, etc.); Computation of characteristics of simple devices (p-n junction, MOS capacitor, MOSFET, etc.); Small-signal analysis.

	Total Periods	**45**

REFERENCES:

1.	L.O.Chua and P.M.Lin, Computer aided analysis and electronic circuits, Prentice Hall, 1975.
2.	S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer-Verlag, 1984
3.	N.J. McCalla, Fundamentals of Computer Aided Circuit Simulation, Kluwer Academic Publishers, 1988.

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		L	T	P	C	CA	ESE	Total
P14VDE07	**SYSTEM DESIGN**	3	0	0	3	50	50	100

Objective	• To study about DSP algorithms. Signal integrity • To study high speed behaviour of interconnects

Basics of system hardware design. Hierarchical design using top-down and bottom-up methodology. System partitioning techniques, interfacing between system components. Handling multiple clock domains, Synchronous and asynchronous design styles. Interface between synchronous and asynchronous blocks. Meta-stability and techniques for handling it. Interfacing linear and digital systems, data conversion circuits. Design of finite state machines, state assignment strategies. Design and optimization of pipelined stages. Use of data flow graphs, Critical path analysis, retiming and scheduling strategies for performance enhancement. Implementation of DSP algorithms. Signal integrity and high speed behaviour of interconnects: ringing, cross talk and ground bounce. Layout strategies at IC and board level for local and global signals. Power supply decoupling; Test strategies: Border Scan, Built In Self Test and signature analysis.

Total Periods	**45**

REFERENCES:

1.	Jan M. Rabaey, "Digital Integrated Circuits", Prentice Hall of India, (New Delhi), 1997.
2.	M.J.S. Smith, "Application Specific Integrated Circuits", Addison Wesley (Reading, MA), 1999.
3.	Vijay K. Madisetti, "VLSI Digital Signal Processing", IEEE Press (NY, USA), 1995

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE08	**INTRODUCTION TO MEMS**	3	0	0	3	50	50	100

Objective	• To study about Micro sensors • To study Thermal micro-actuation • To study DNA-chip, micro-arrays

Historical Background: Silicon Pressure sensors, Micromachining, Micro Electro Mechanical Systems; Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA);Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors; Microactuators : Electromagnetic and Thermal micro actuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector; Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems: Success Stories, Micromotors, Gear trains, Mechanisms; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays; Lab/Design:(two groups will work on one of the following design project as a part of the course).;RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.

	Total Periods	**45**

REFERENCES:

1.	Stephen D. Senturia, "Microsystem Design" by, Kluwer Academic Publishers, 2001.Marc Madou
2.	Fundamentals of Microfabrication by, CRC Press, 1997.Gregory Kovacs, Micromachined Transducers Sourcebook WCB McGraw-Hill, Boston, 1998
3.	M.-H. Bao, Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes by Elsevier, New York, 2000

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE09	**TESTING AND VERIFICATION OF VLSI CIRCUITS**	3	0	0	3	50	50	100

Objectives	• To study about verification in VLSI design process • To study different level of SOC • To modeling of BIST for testing

Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs; Fundamentals of VLSI testing. Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan. System testing and test for SOCs. IDDQ testing. Delay fault testing. BIST for testing of logic and memories. Test automation; Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

Total Periods	**45**

REFERENCES:

1.	M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000
2.	M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.
3.	T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000
4.	P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE10	**ADVANCED NETWORK ANALYSIS**	3	0	0	3	50	50	100

Objective	• To study about Theorems of Tellegen • To study different level of networks and systems

Matrices associated with graphs, the short circuit and open circuit operations, their generalization through the use of ideal transformers and vector space operations corresponding to these operations. Theorems of Tellegen and Minty: Formal equivalence, areas of applications. The Implicit Duality Theorem and its applications: Multiport decomposition, ideal transformer resulting from the connection of ideal transformers, adjoint networks and systems, networks with decomposition methods based on altering network topology, ideal diode, ideal transformer, resistor circuits and their relation to Linear and Quadratic Programming.

Total Periods	**45**

REFERENCES:

1.	S.Seshu and M.B.Reed, Linear Graphs and Electrical Networks, Addison Wesley, 1961.
2.	H.Narayanan, Submodular Functions and Electrical Networks, Annals of Discrete Maths, vol-54, North Holland, 1997.

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Department	**APLLIED ELECTRONICS & VLSI DESIGN / ELECTRONICS AND COMMUNICATION ENGINEERING**		Semester		

Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE11	**EMBEDDED SYSTEMS DESIGN**	3	0	0	3	50	50	100

Objective	• To study embedded systems design • To study different level of Design trade offs

The concept of embedded systems design. Embedded microcontroller cores, embedded memories. Examples of embedded systems; Technological aspects of embedded systems: interfacing between analog and digital blocks, signal conditioning, digital signal processing. Sub-system interfacing, interfacing with external systems, user interfacing. Design tradeoffs due to process compatibility, thermal considerations, etc; Software aspects of embedded systems: real time programming languages and operating systems for embedded systems.

Total Periods	**45**

REFERENCES:

1.	J.W. Valvano, "Embedded Microcomputer System: Real Time Interfacing", Brooks/Cole, 2000.
2.	Jack Ganssle, "The Art of Designing Embedded Systems", Newnes, 1999
3.	V.K. Madisetti, "VLSI Digital Signal Processing", IEEE Press (NY, USA), 1995
4.	David Simon, "An Embedded Software Primer", Addison Wesley, 2000.
5.	K.J. Ayala, "The 8051 Microcontroller: Architecture, Programming, and Applications", Penram Intl, 1996.

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Course Code	Course Name	Periods Per Week			Credit	Maximum Marks		
		L	T	P	C	CA	ESE	Total
P14VDE12	**MIXED SIGNAL VLSI DESIGN**	3	0	0	3	50	50	100

Objective	• To study about Basics of Analog to digital converters • To study High-speed ADCs

Prerequisite: EE618.;Review of continuous-time filters, Discrete-time filters, Analog and discrete-time signal processing, Analog integrated continuous-time and discrete-time (switched-capacitor) filters; Basics of Analog to digital converters (ADC), Basics of Digital to analog converters (DAC), DACs, Successive approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters)Mixed-Signal layout, Interconnects, Phase locked loops, Delay locked loops.

Total Periods	**45**

REFERENCES:

1.	CMOS mixed-signal circuit design by R. Jacob Baker, Wiley India, IEEE press, reprint 2008.
2.	Design of analog CMOS integrated circuits by Behzad Razavi, McGraw-Hill, 2003
3.	CMOS circuit design, layout and simulation by R. Jacob Baker, Revised second edition, IEEE press, 2008.
4.	CMOS Integrated ADCs and DACs by Rudy V. dePlassche, Springer, Indian edition, 2005.
5.	Electronic Filter Design Handbook by Arthur B. Williams, McGraw-Hill, 1981
6.	Design of analog filters by R. Schauman, Prentice-Hall 1990 (or newer additions).
7.	An introduction to mixed-signal IC test and measurement by M. Burns et al., Oxford university press, first Indian edition, 2008.